Department of Electrical Engineering, Feng-Chia University

Chapter 1
Computer Abstractions and Technology (Part 1)

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Outline

- Introduction
- Computer Software & Hardware
- Processor Trends
- IC Design and Manufacture

What is a computer?

- Components:
  - Input (mouse, keyboard)
  - Output (display, printer)
  - Memory (disk drives, DRAM, SRAM, CD)
  - Network

- Our primary focus : the processor (datapath and control)
  - Learn instruction set design for RISC processor
  - Learn the basic hardware that can implement these instructions
  - Learn the different ways that control the processor
  - Learn the performance enhancing techniques
  - Learn the system concept you need in an SoC system

Text Book : P5

Computer markets

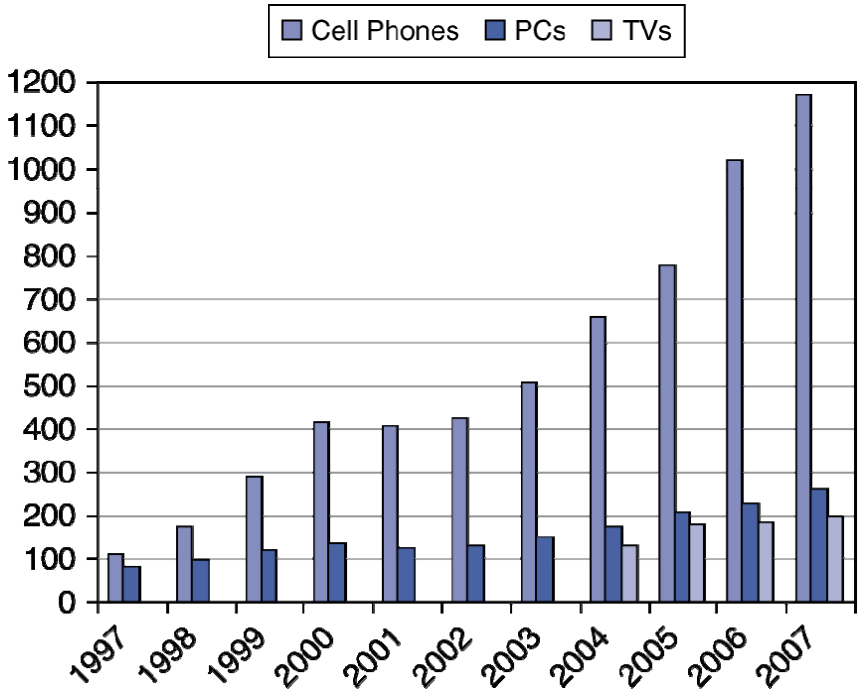
- Desktop computers
  - Cost/performance tradeoff

- Servers
  - Availability
  - Scalability
  - Efficient throughput

- Embedded computers
  - Real time performance (soft deadline and hard deadline)
  - Minimize power and minimize memory size

Text Book : P6

The Processor Market



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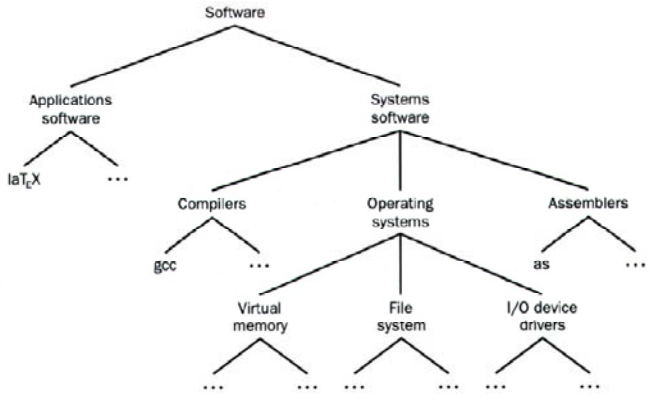
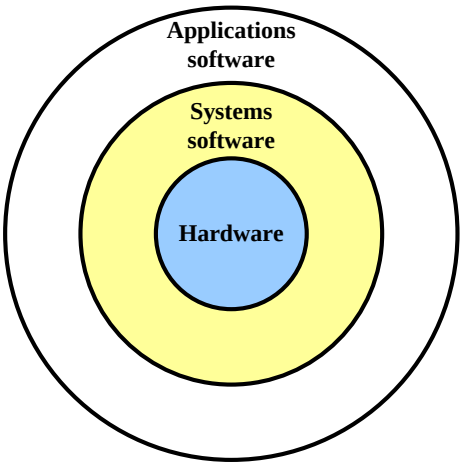
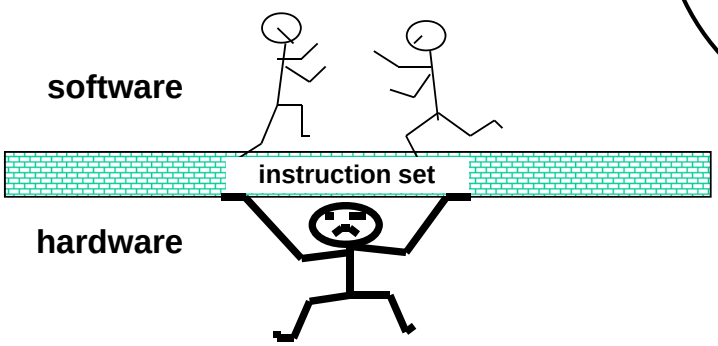
Text Book : P10

Abstraction of layers

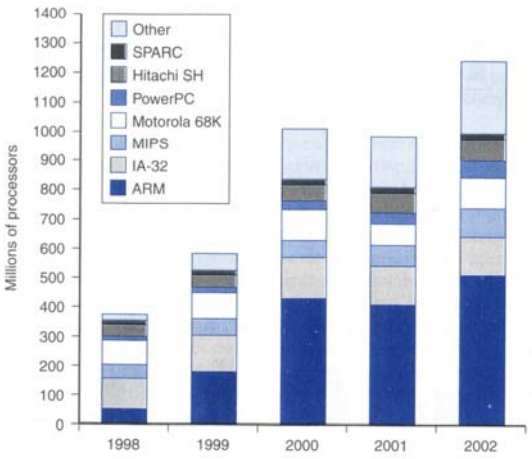






Instruction Set Architecture (ISA)

- A very important abstraction
  - Interface between hardware and low-level software
  - Standardizes instructions, machine language bit patterns, etc.
  - Advantage: *different implementations of the same architecture*
  - Disadvantage: *sometimes prevents using new innovations*
- Modern instruction set architectures:
  - ARM
  - IA-32 (x86)
  - MIPS
  - PowerPC
  - SPARC
  - Others



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Architecture vs. Organization

Computer Architecture

- Instruction set architecture
  - Programmer-visible instruction set
- Organization
- Hardware
  - VLSI circuit, Packaging, Power etc.

Computer Organization

- Operational units and their interconnections
  - Memory system, bus, ALU, pipeline…
- Same instruction but different organization

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Text Book : P11 ~ P13, & App.B

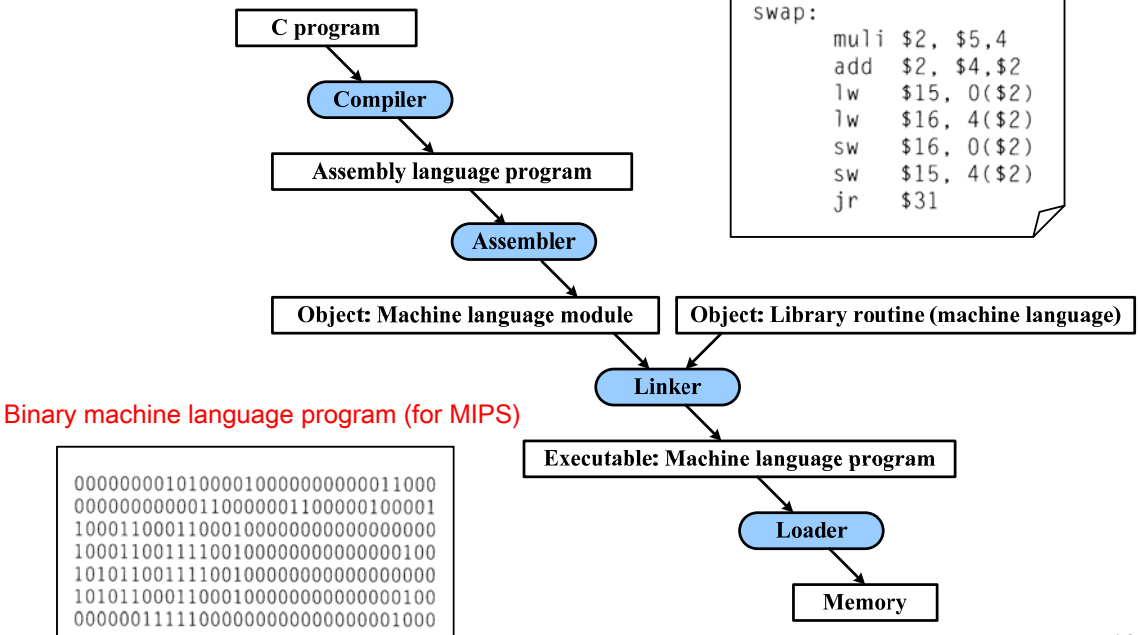
High-level language program (in C)

```
swap(int v[], int k)
{int temp;
   temp = v[k];
   v[k] = v[k+1];
   v[k+1] = temp;
}
```

An abstraction omits unneeded detail, helps us cope with complexity

Assembly language program (for MIPS)

```
swap:
        muli $2, $5,4
        add  $2, $4,$2
        lw   $15, 0($2)
        lw   $16, 4($2)
        sw   $16, 0($2)
        sw   $15, 4($2)
        jr   $31
```

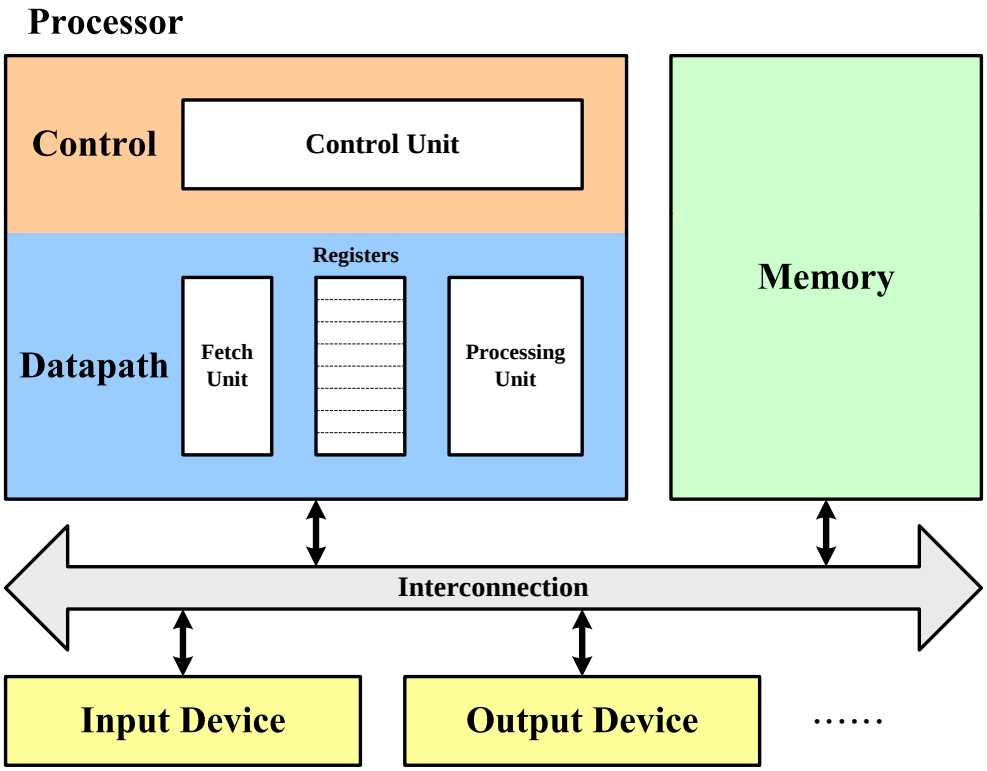


Binary machine language program (for MIPS)

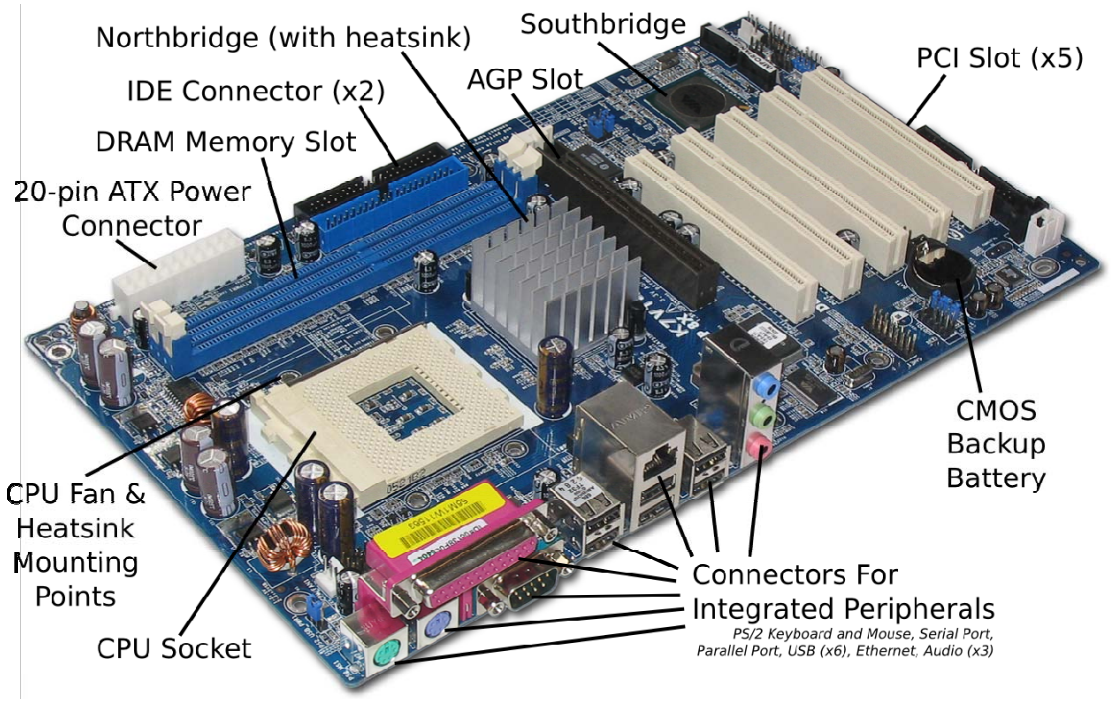
```
00000000101000010000000000011000
00000000000110000011000001000001
10001100011000100000000000000000
10001100111100100000000000000100
10101100111100100000000000000000
10101100011000100000000000000100
00000011111000000000000000001000
```

Text Book : P14

The 5 classic components of a computer

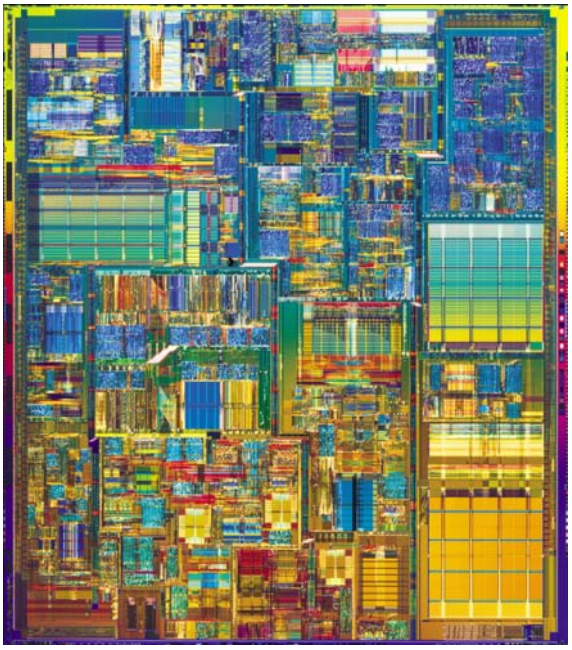


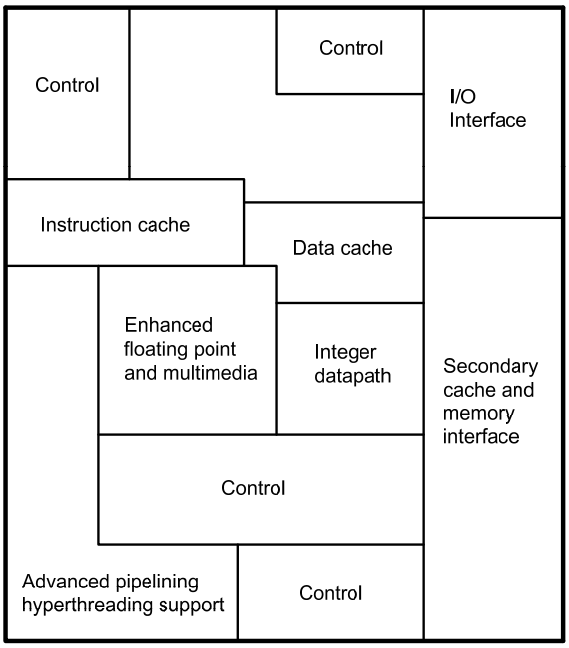
Motherboard



Source : http://en.wikipedia.org/wiki/Motherboard

Processor Chip





Source : http://www.tayloredge.com/museum/processor/processorhistory.html

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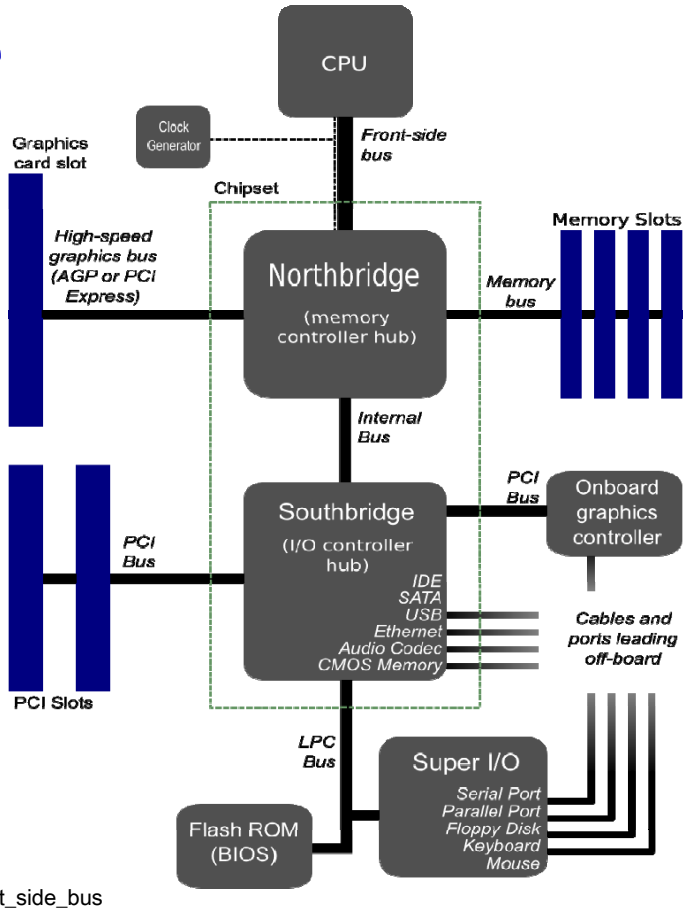
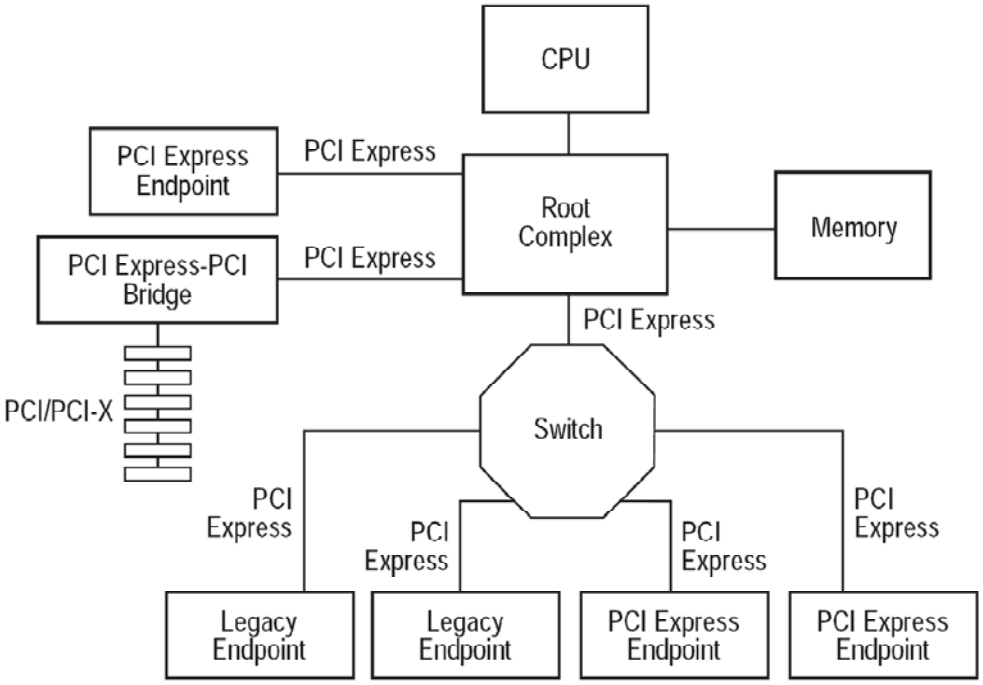
Desktop PC



Source : http://en.wikipedia.org/wiki/Front_side_bus

PCI Express System



Source : PCI Express™ Base Specification Revision 1.0a

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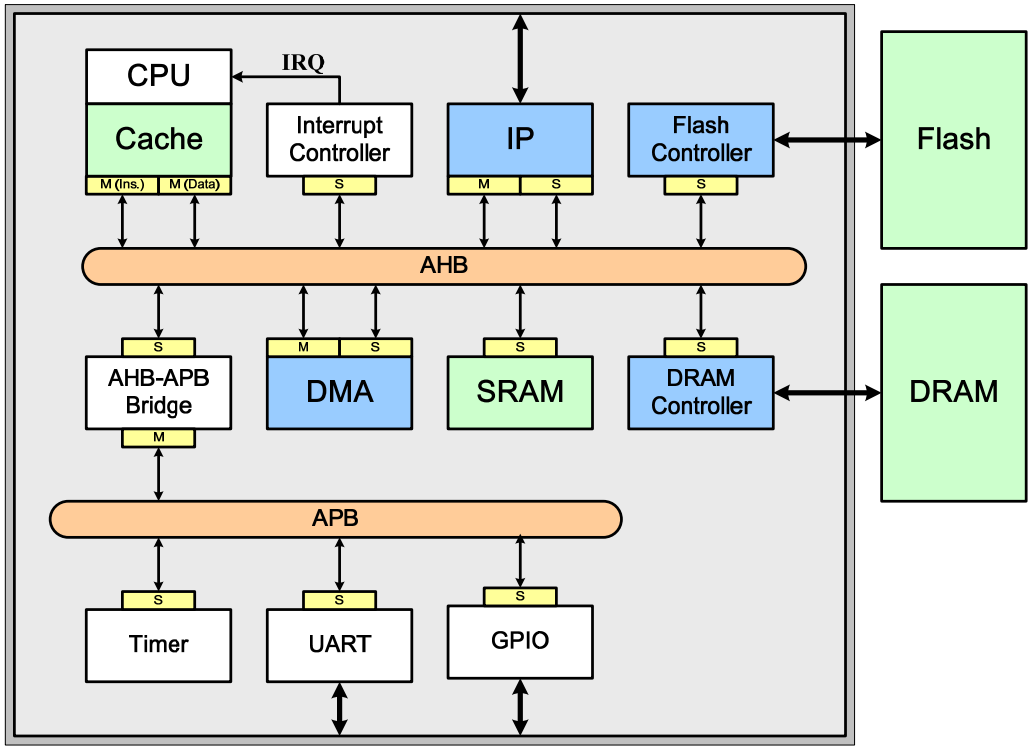
System on a Chip (SoC)



A Safe Place for Data

- Volatile main memory
  - Loses instructions and data when power off
- Non-volatile secondary memory
  - Magnetic disk
  - Flash memory
  - Optical disk (CDROM, DVD)

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Text Book : P41 ~ P42

Uniprocessor Performance

Gordon Moore
Intel Cofounder
B.S. Cal 1950!

2X Transistors / Chip
Every 1.5 years
Called "Moore's Law"

- Constrained by power, instruction-level parallelism, memory latency

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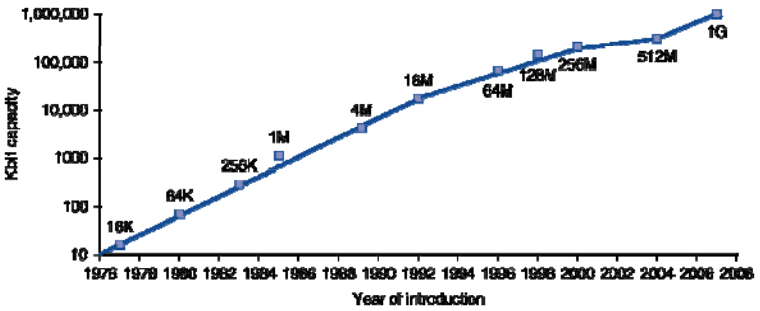
Text Book : P25 ~ P26

Technology Trends

- Electronics technology continues to evolve
  - Increased capacity and performance
  - Reduced cost

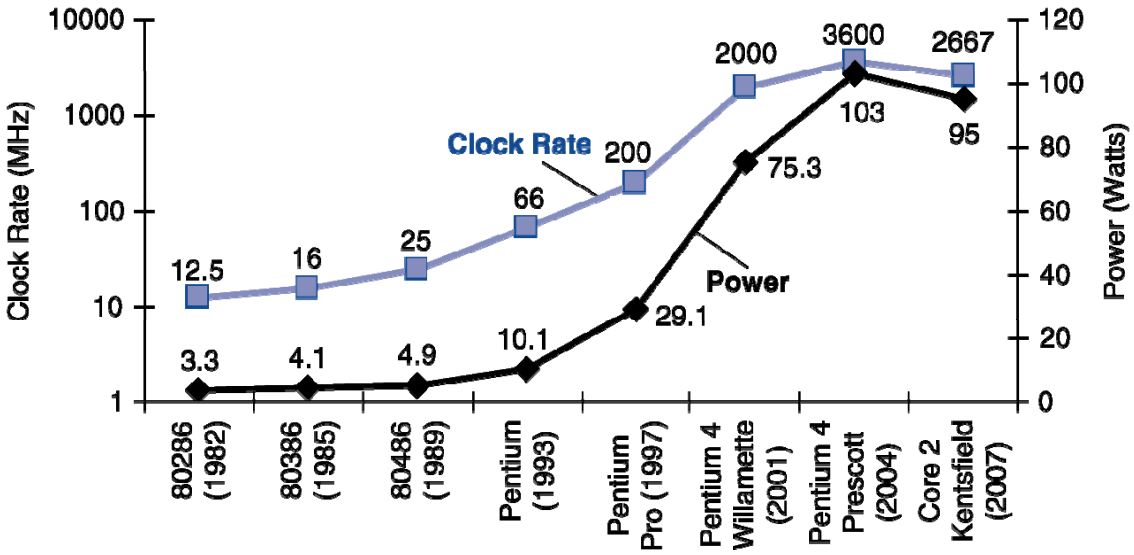
DRAM capacity



Year	Technology	Relative performance/cost
1951	Vacuum tube	1
1965	Transistor	35
1975	Integrated circuit (IC)	900
1995	Very large scale IC (VLSI)	2,400,000
2005	Ultra large scale IC (ULSI)	6,200,000,000

Text Book : P39 ~ P40

Power Trends



- In CMOS IC technology

$$\text{Power} = \text{Capacitive load} \times \text{Voltage}^2 \times \text{Frequency}$$

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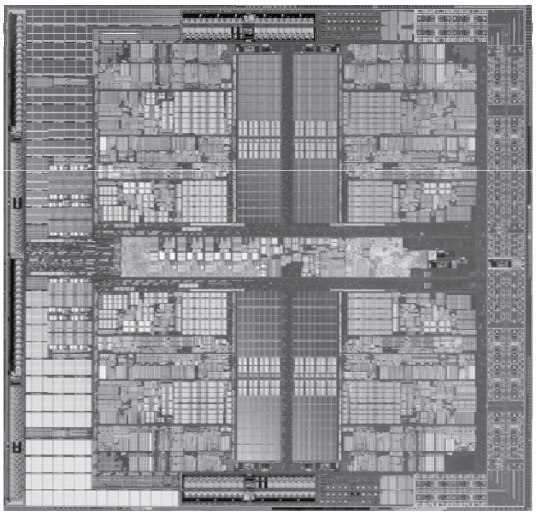
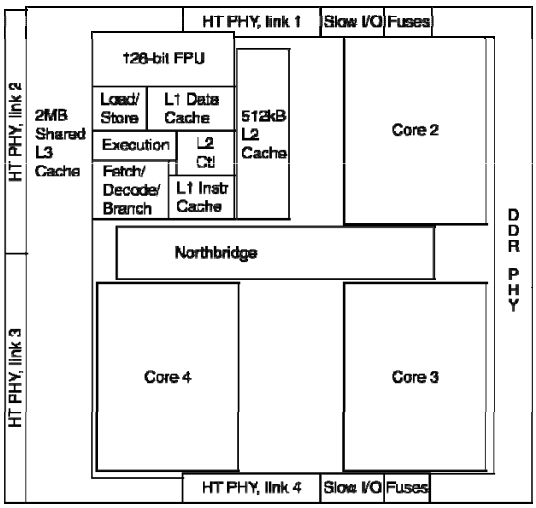
Text Book : P20

Inside the Processor

- AMD Barcelona: 4 processor cores





Text Book : P41 ~ P44

Multiprocessors

- Multicore microprocessors
  - More than one processor per chip
- Requires explicitly parallel programming
  - Compare with instruction level parallelism
    - Hardware executes multiple instructions at once
    - Hidden from the programmer
  - Hard to do
    - Programming for performance
    - Load balancing
    - Optimizing communication and synchronization

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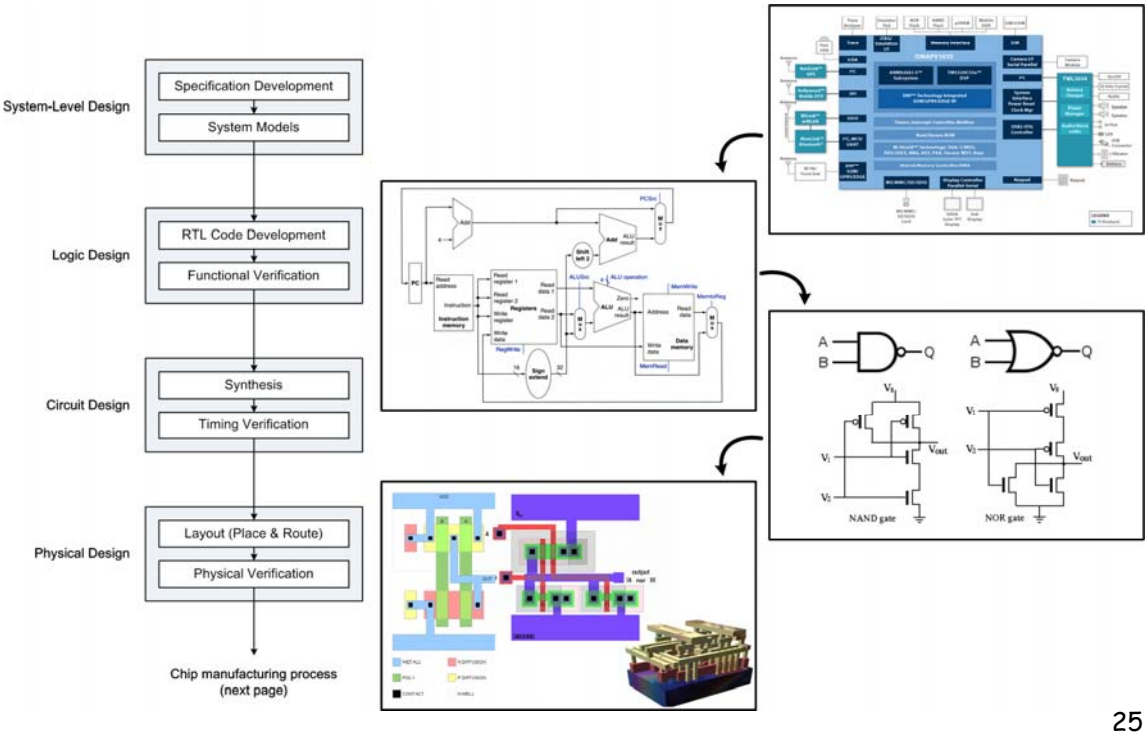
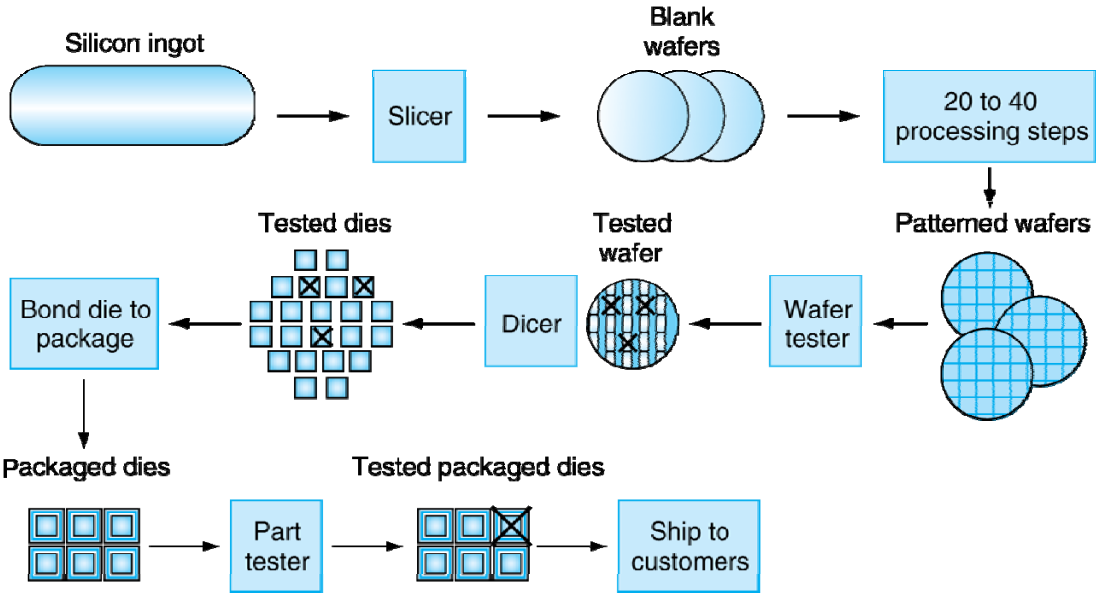
Cell-based IC design flow



Text Book : P44 ~ P46

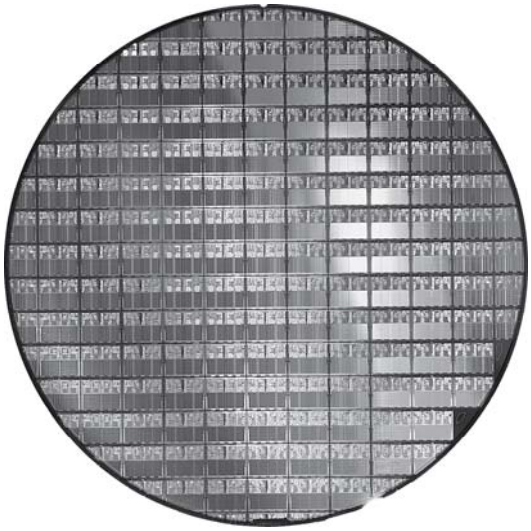
Chip manufacturing process

- Cost of IC = (die + testing + packaging) / final test yield



Text Book : P47

AMD Opteron X2 Wafer



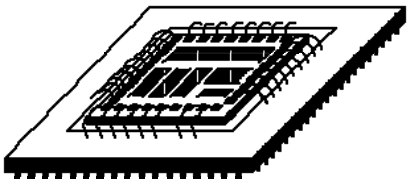
- X2: 300mm wafer, 117 chips, 90nm technology
- X4: 45nm technology

Integrated Circuits (2007 state-of-the-art)

Bare Die

- Primarily Crystalline Silicon
- 1mm - 25mm on a side
- 2007 feature size ~ 65 nm = 65 x 10^{-9} m (then 45, 32, 22, and 16 [by yr 2013])
- 100 - 1000M transistors
- (25 - 100M "logic gates")
- 3 - 10 conductive layers
- "CMOS" (complementary metal oxide semiconductor) - most common.

Chip in Package



- Package provides:
  - spreading of chip-level signal paths to board-level
  - heat dissipation.
- Ceramic or plastic with gold wires.

Source : http://inst.eecs.berkeley.edu/~cs61c