

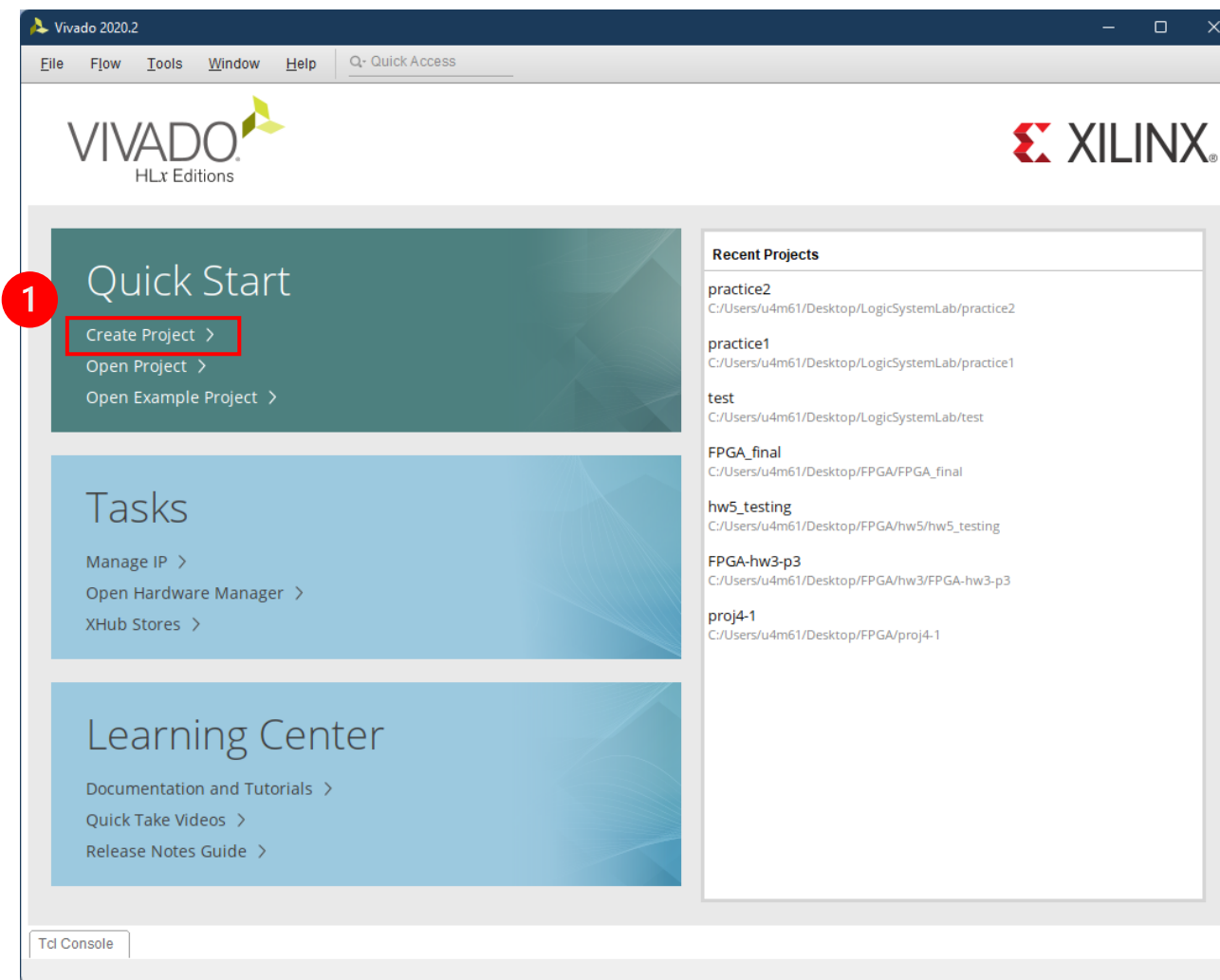
Laboratory 7

PYNQ操作教學

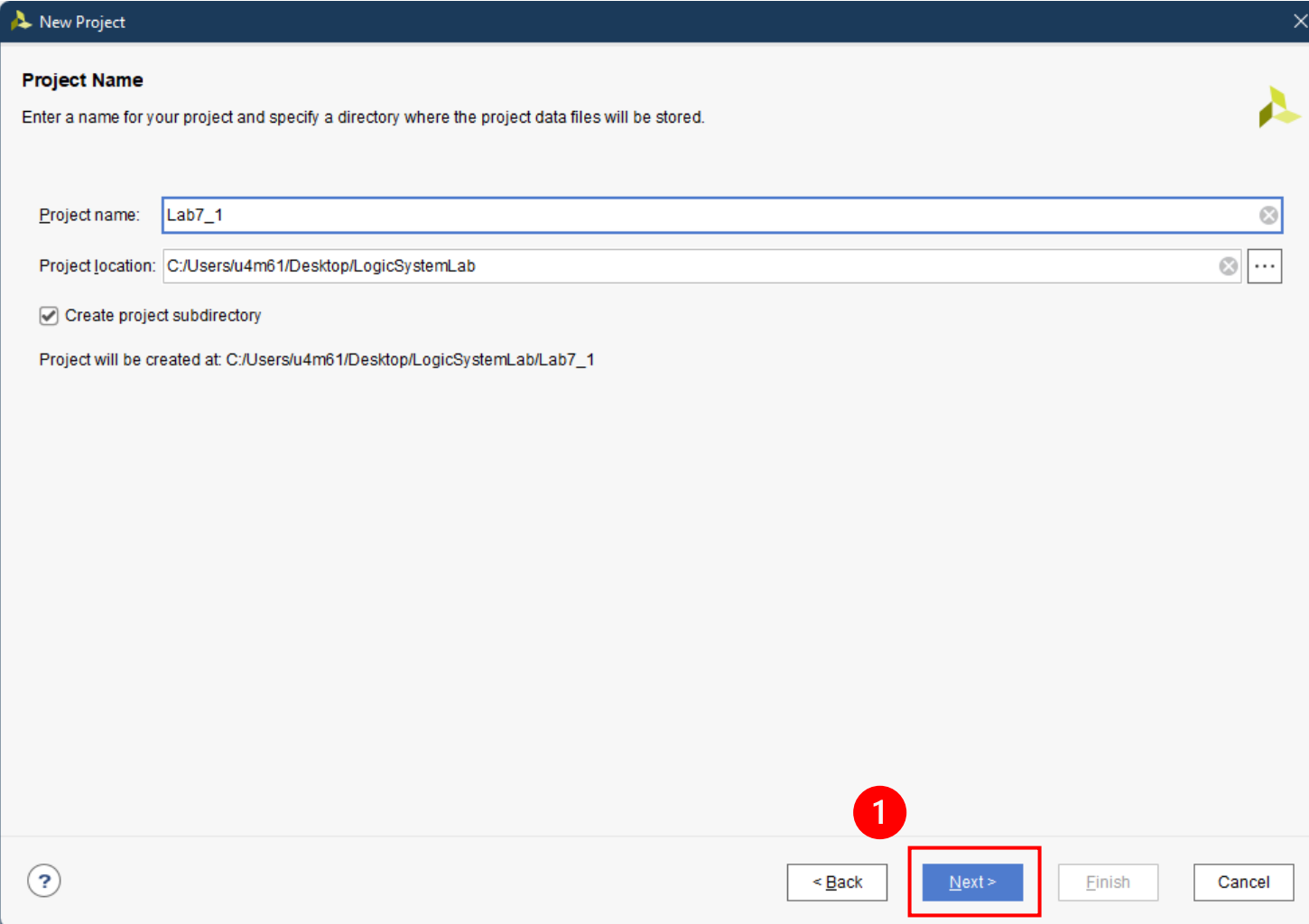


Department of Electrical Engineering
National Cheng Kung University

新增Project



新增Project



The image shows a 'New Project' dialog box with a dark blue title bar. The main area is light gray. At the top, it says 'Project Name' and 'Enter a name for your project and specify a directory where the project data files will be stored.' Below this, there are two text input fields. The first is labeled 'Project name:' and contains the text 'Lab7_1'. The second is labeled 'Project location:' and contains the text 'C:/Users/u4m61/Desktop/LogicSystemLab'. To the right of the second field is a button with three dots. Below the fields, there is a checkbox labeled 'Create project subdirectory' which is checked. Below the checkbox, it says 'Project will be created at: C:/Users/u4m61/Desktop/LogicSystemLab/Lab7_1'. At the bottom, there are four buttons: '< Back', 'Next >', 'Finish', and 'Cancel'. The 'Next >' button is highlighted with a red rectangle and a red circle with the number '1' next to it. There is also a help icon (a question mark in a circle) on the bottom left.

New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name: Lab7_1

Project location: C:/Users/u4m61/Desktop/LogicSystemLab

☒ Create project subdirectory

Project will be created at: C:/Users/u4m61/Desktop/LogicSystemLab/Lab7_1

? < Back Next > Finish Cancel

新增Project

New Project

Project Type
Specify the type of project to create.

1

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☒ Do not specify sources at this time
☐ Project is an extensible Vitis platform

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

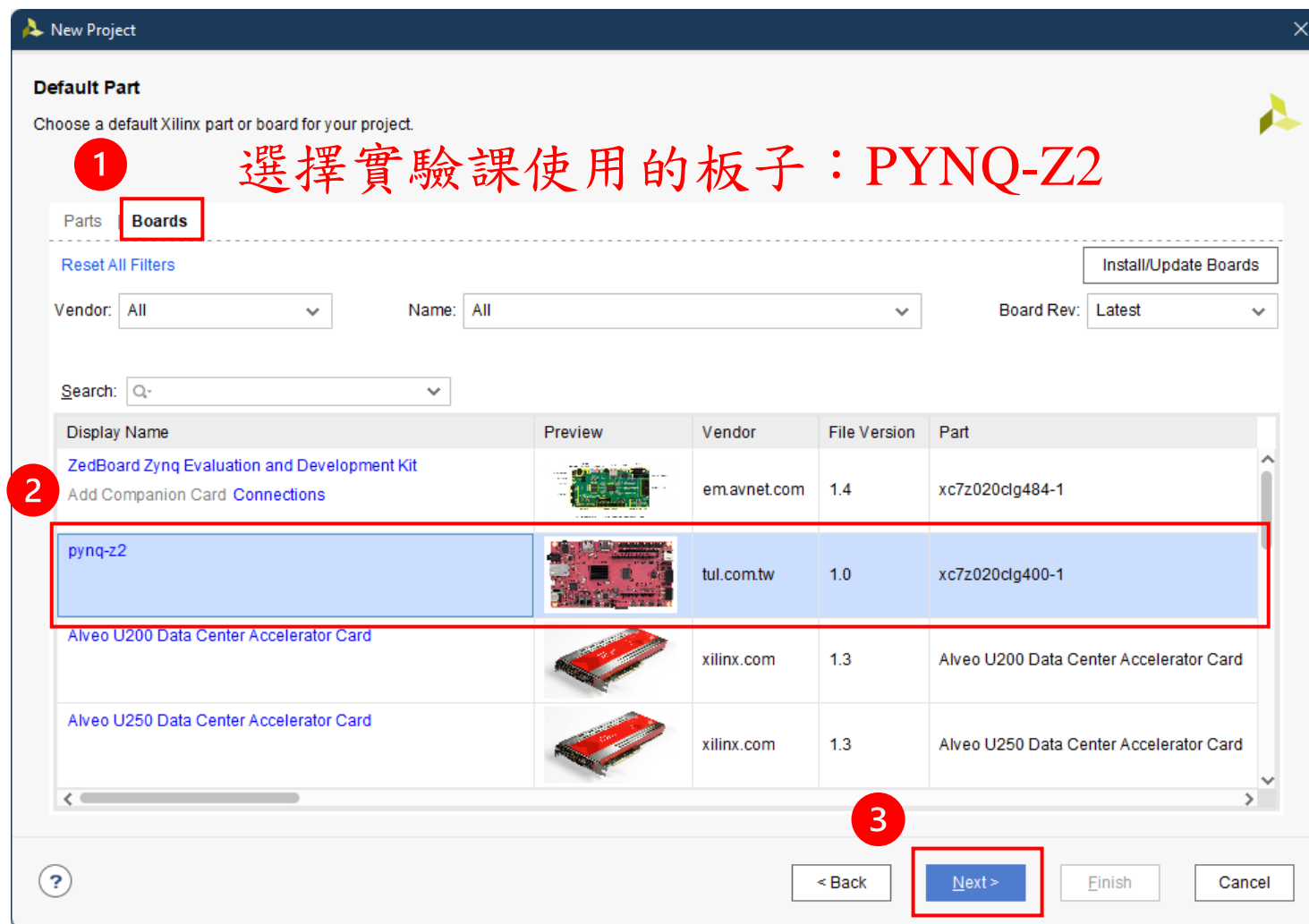
☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

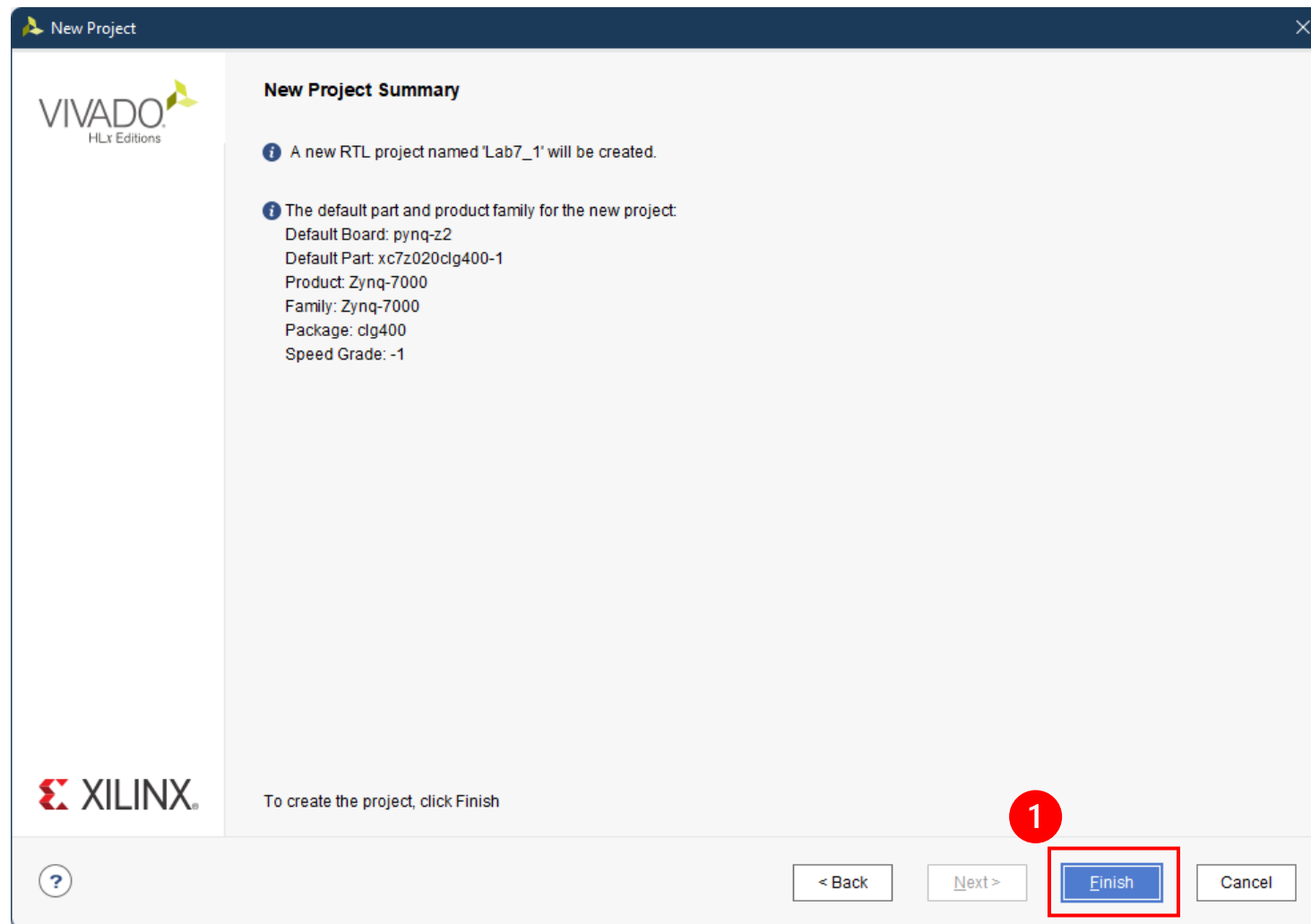
2

? < Back Next > Finish Cancel

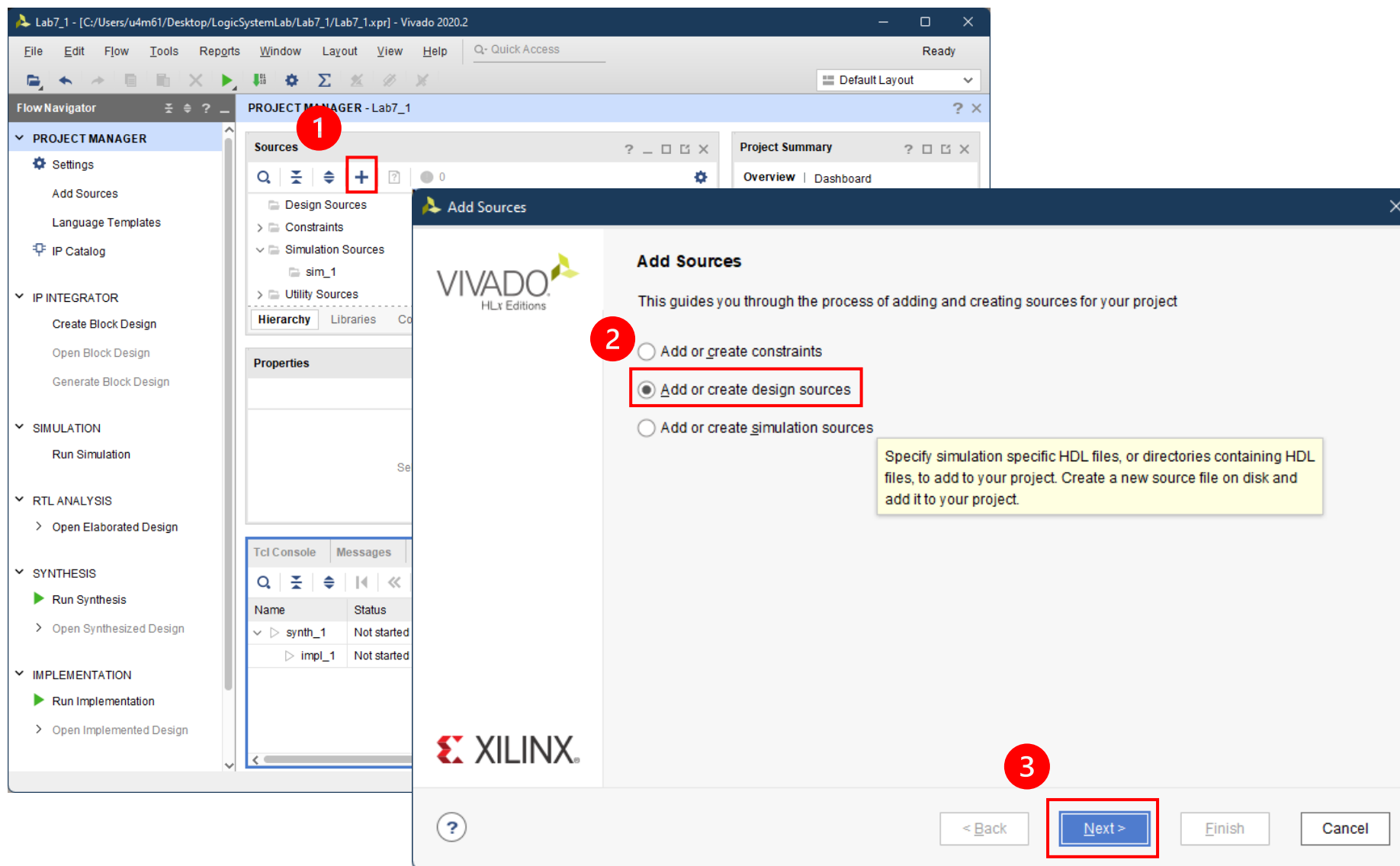
新增Project



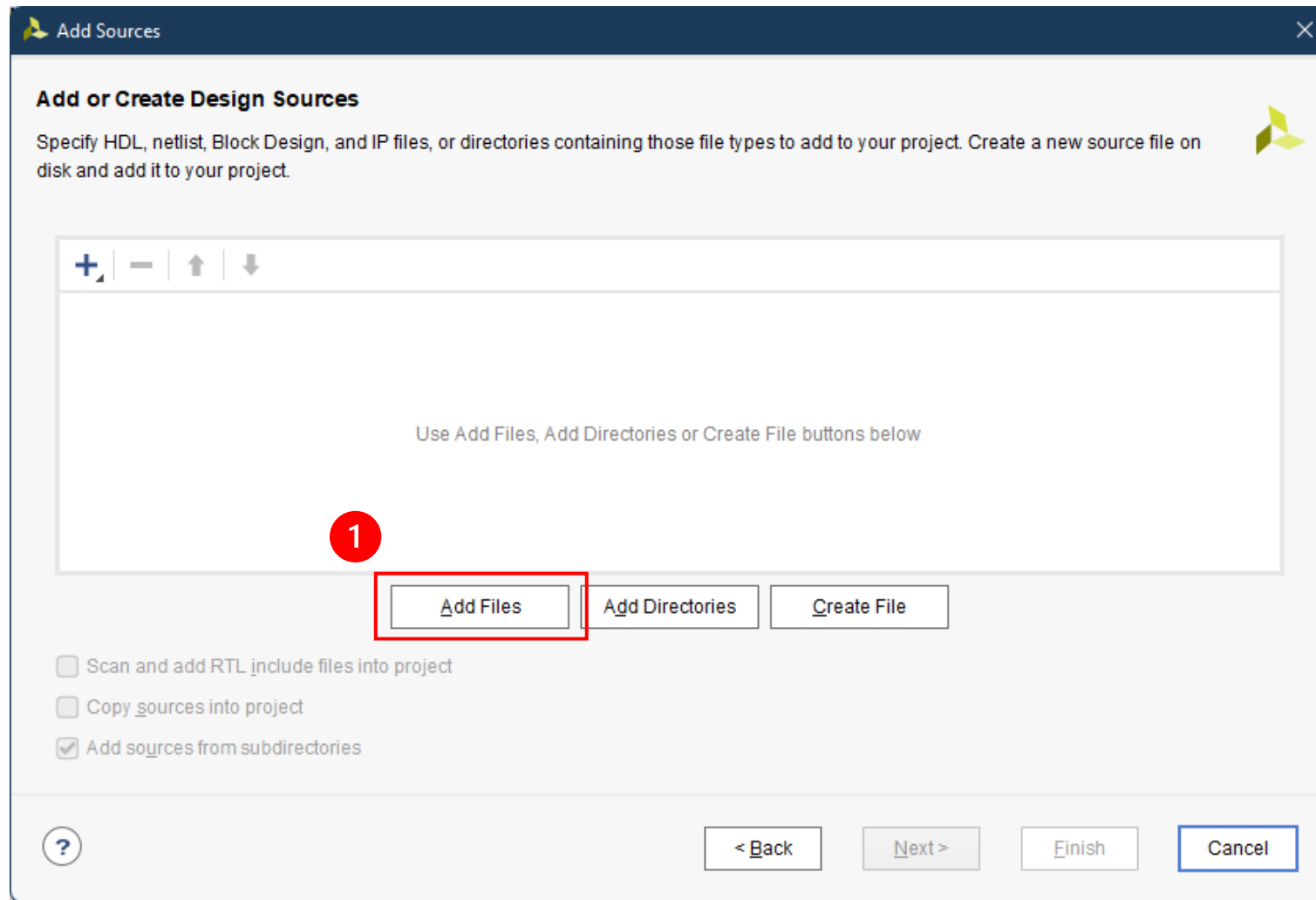
新增Project



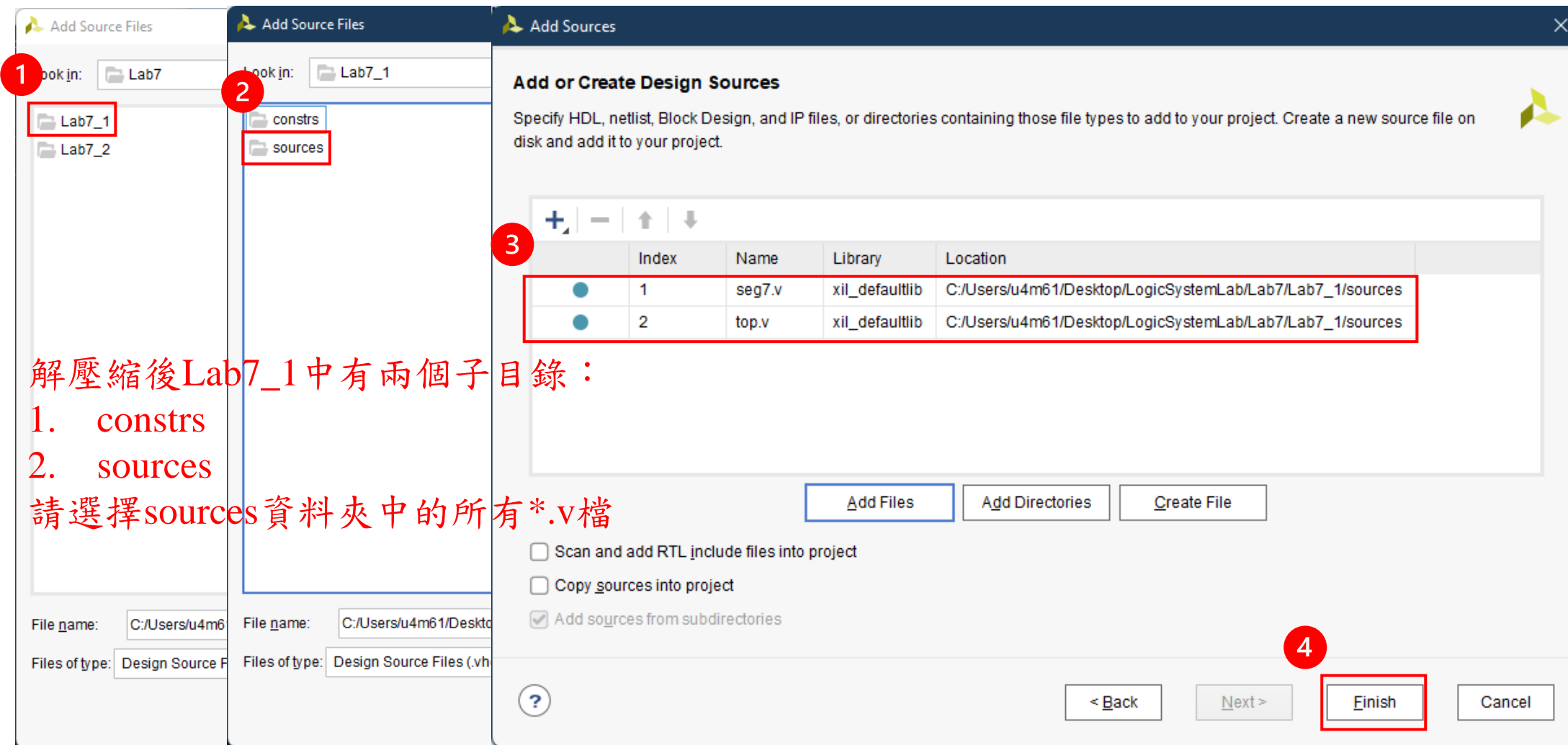
加入 Verilog Source



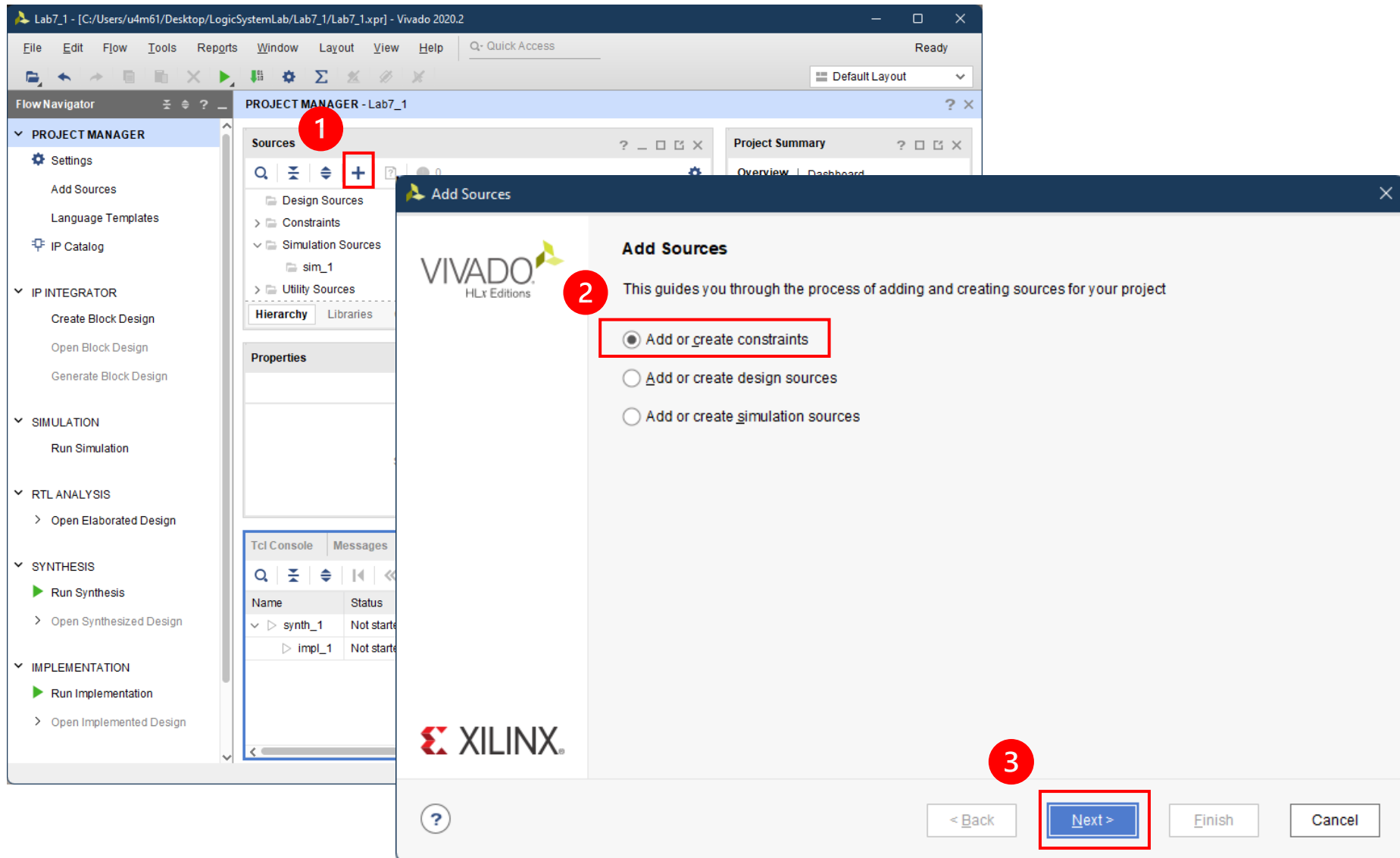
加入 Verilog Source



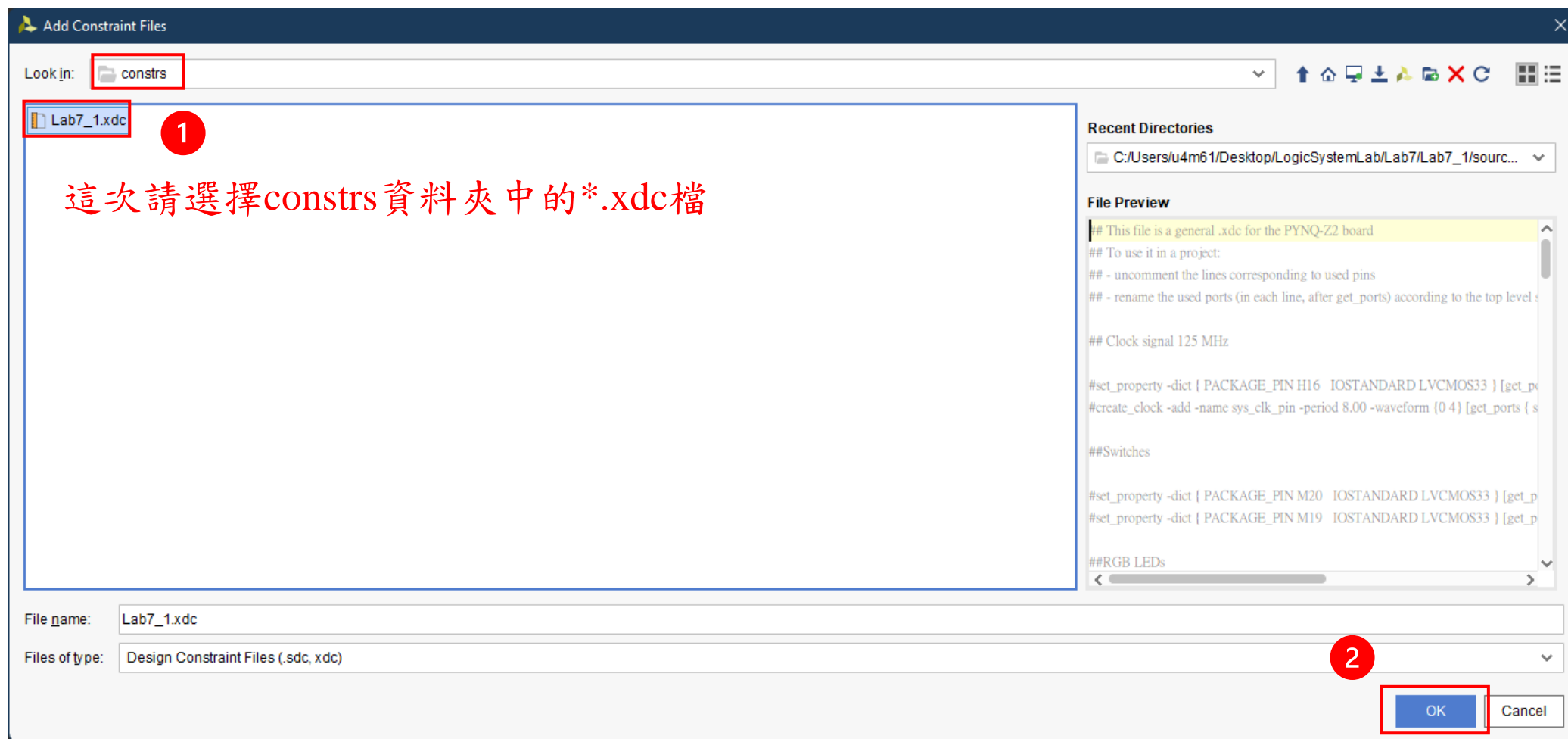
加入 Verilog Source



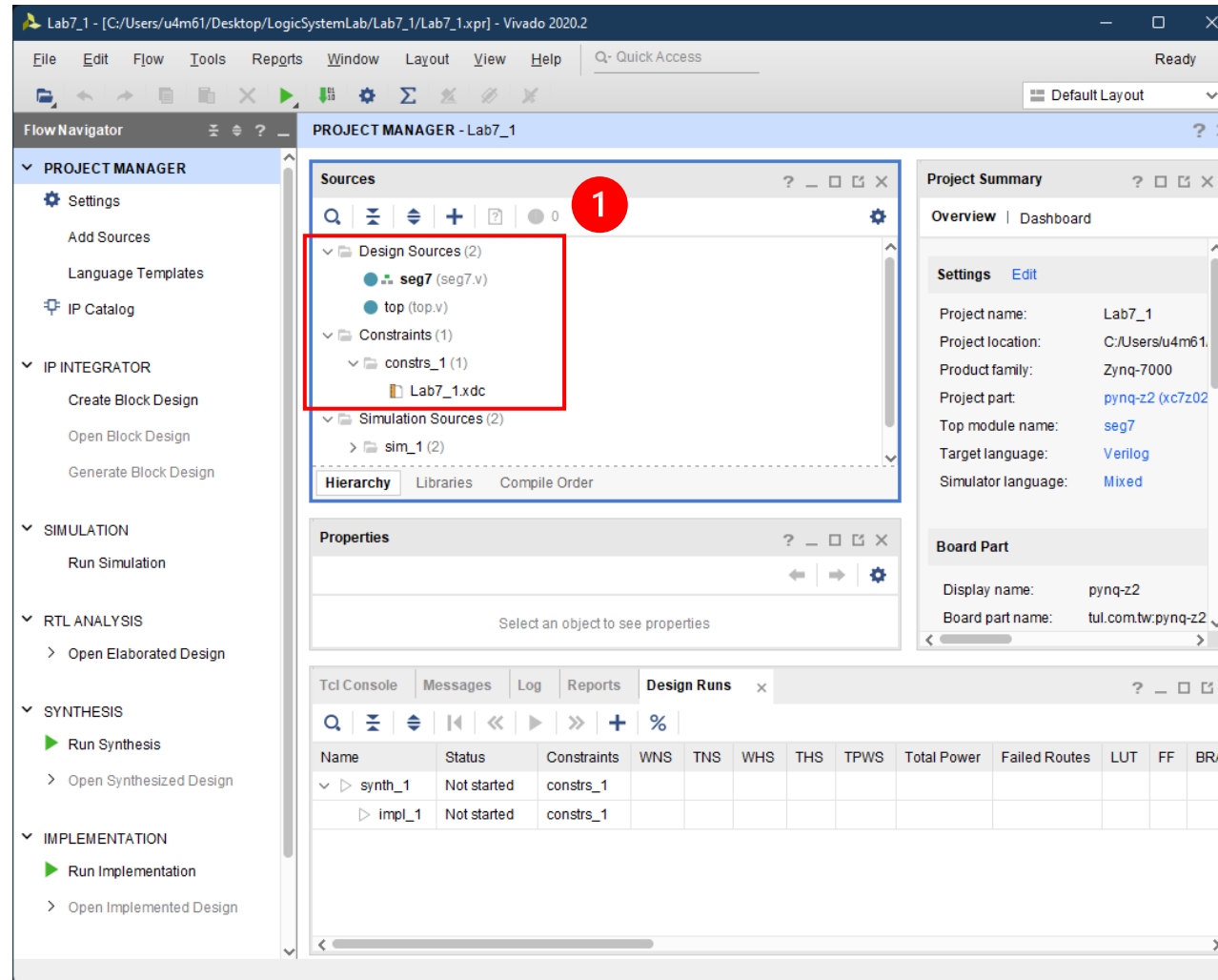
加入PYNQ Constraint



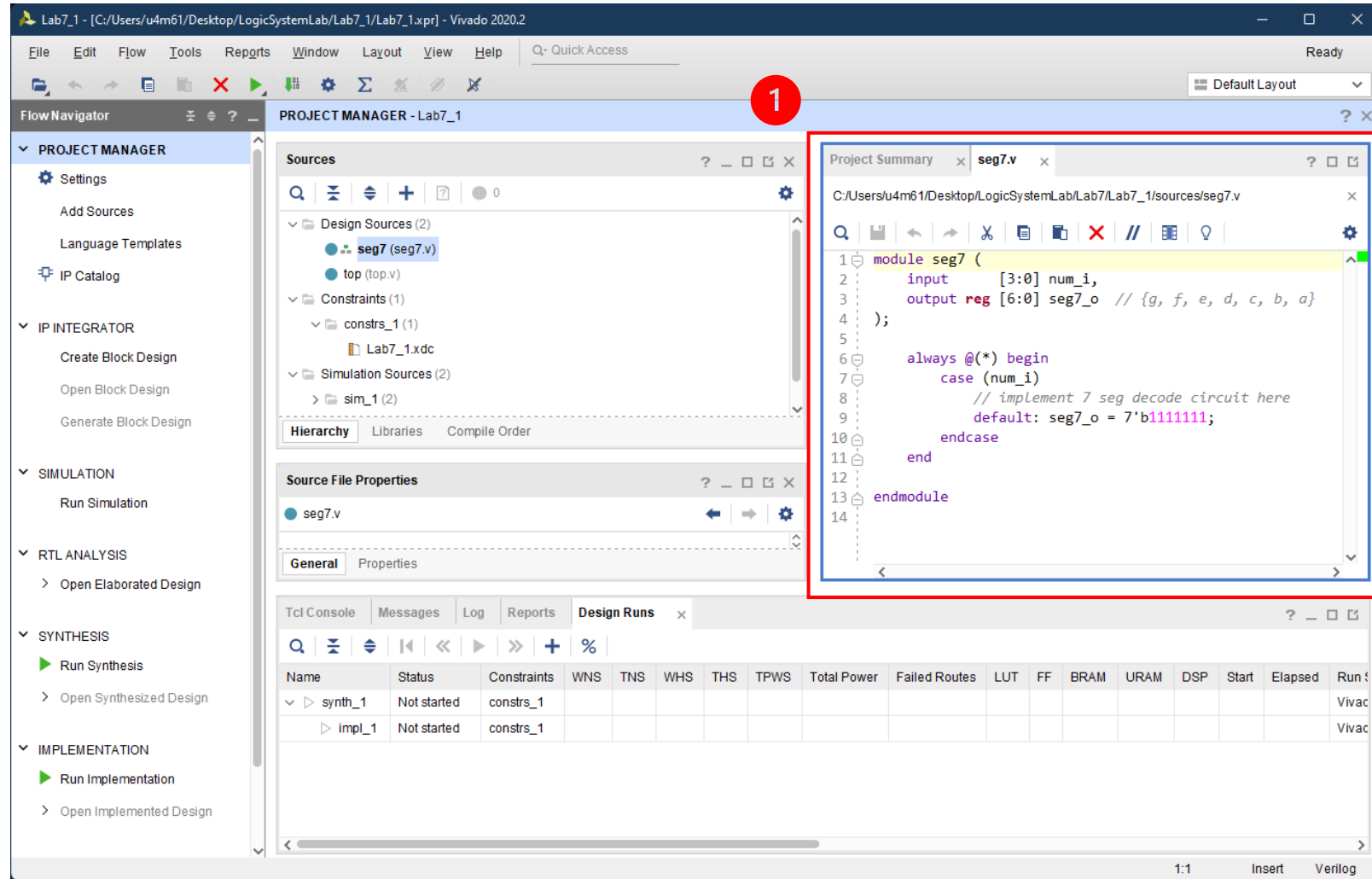
加入PYNQ Constraint



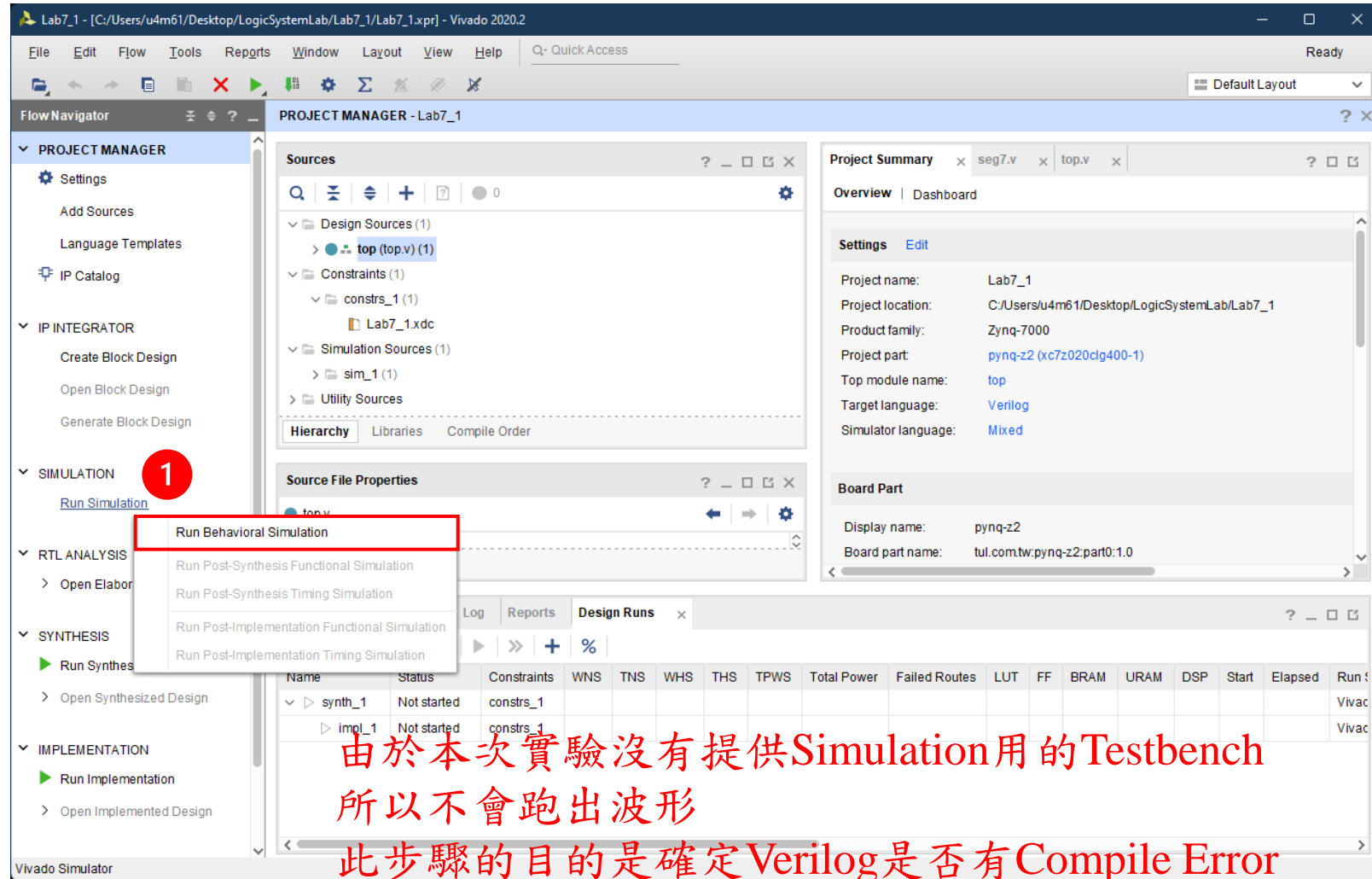
確定檔案成功加入Project



編輯 Verilog 檔案



可以先Run Simulation確認有無錯誤



Run Synthesis

開始Run Synthesis後會看到
Vivado右上角有正在合成的提示

1

2

3

Running synth_design Cancel

Default Layout

Launch Runs

Launch the selected synthesis or implementation runs.

Launch directory: <Default Launch Directory>

Options

☒ Launch runs on local host Number of jobs: 6

☐ Generate scripts only

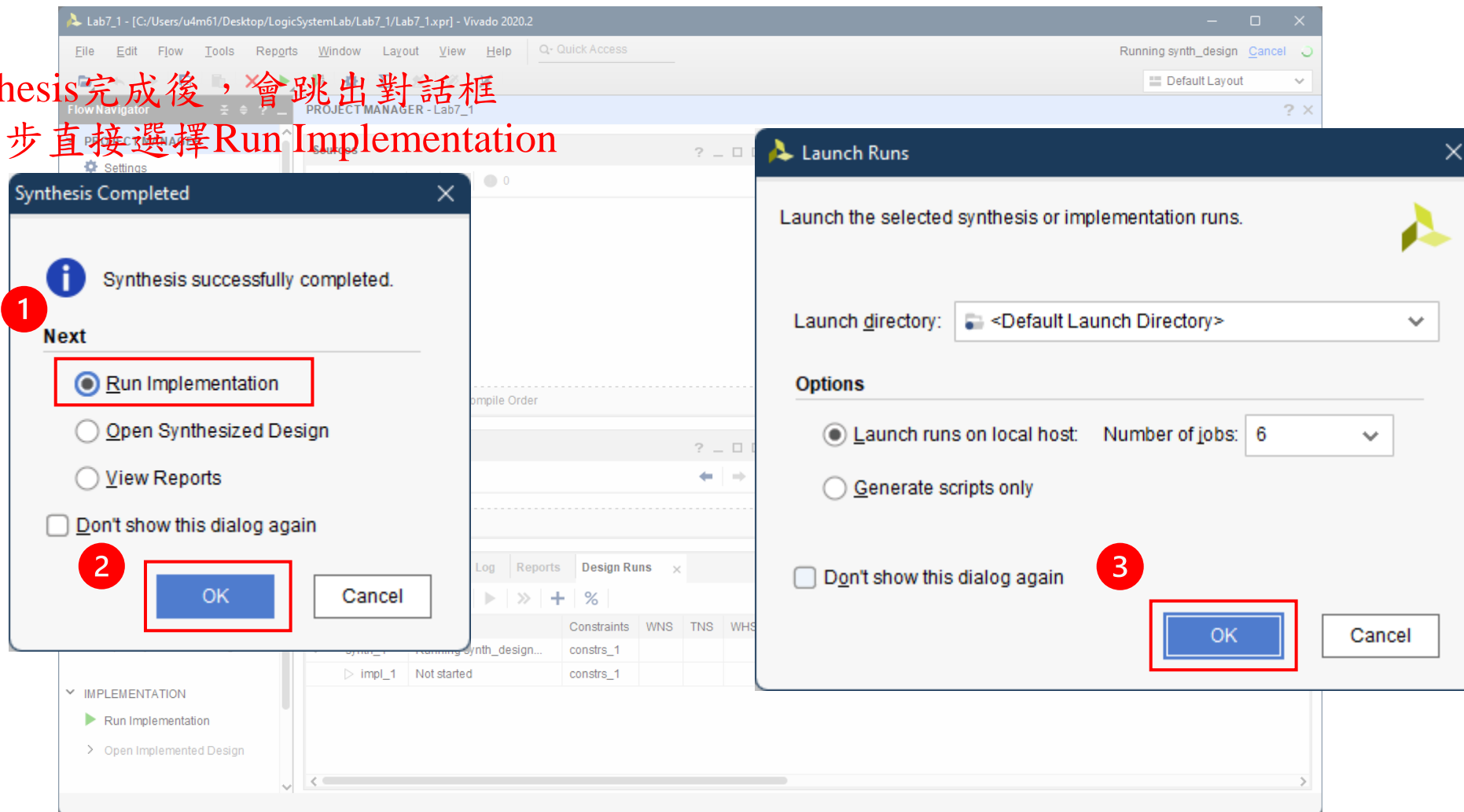
☐ Don't show this dialog again

OK Cancel

Name	Status	Constraints	WNS	TNS	WHS	THS	TPWS
synth_1	Not started	constrs_1					
impl_1	Not started	constrs_1					

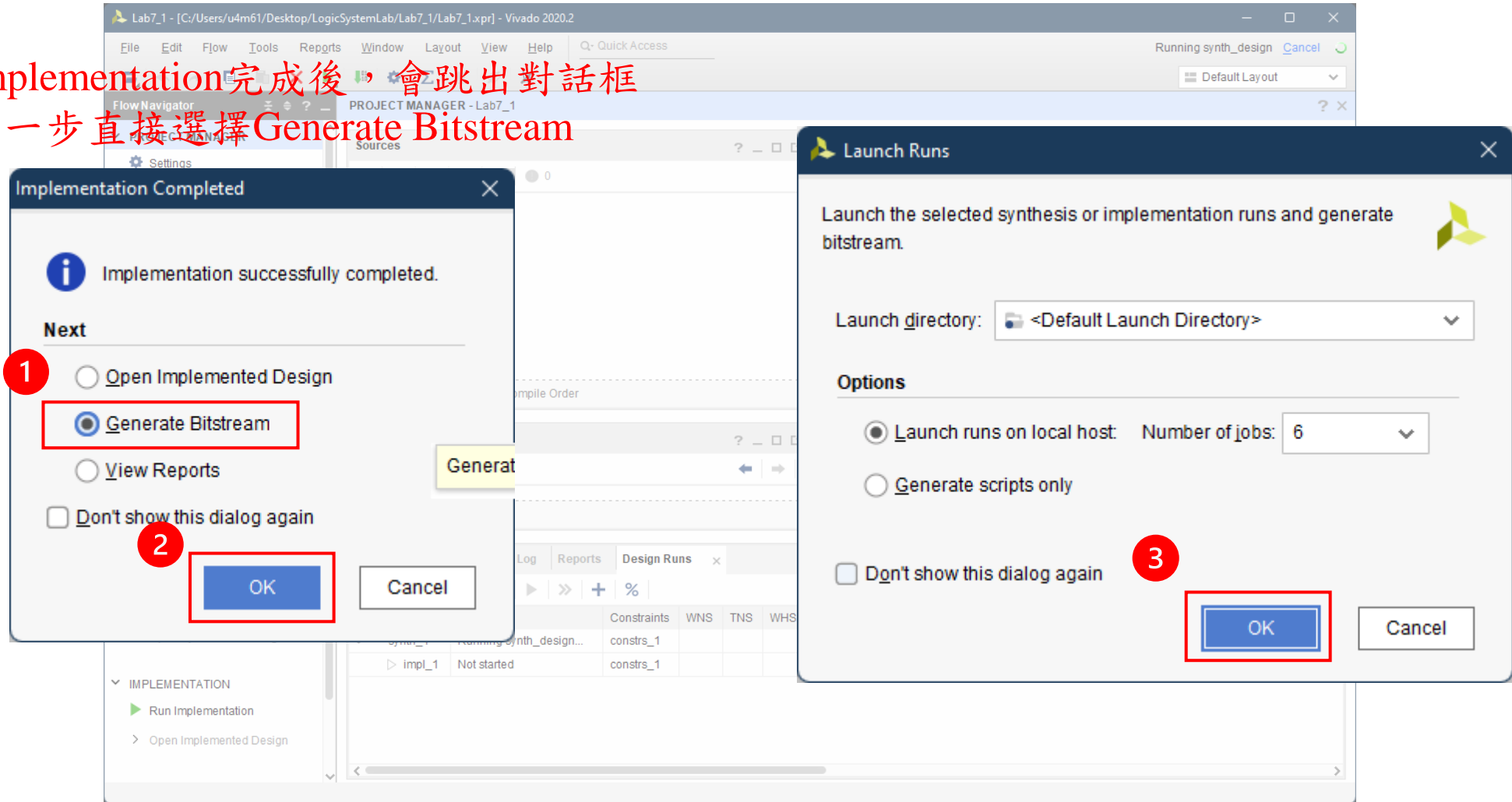
Run Implementation

Synthesis完成後，會跳出對話框
下一步直接選擇Run Implementation

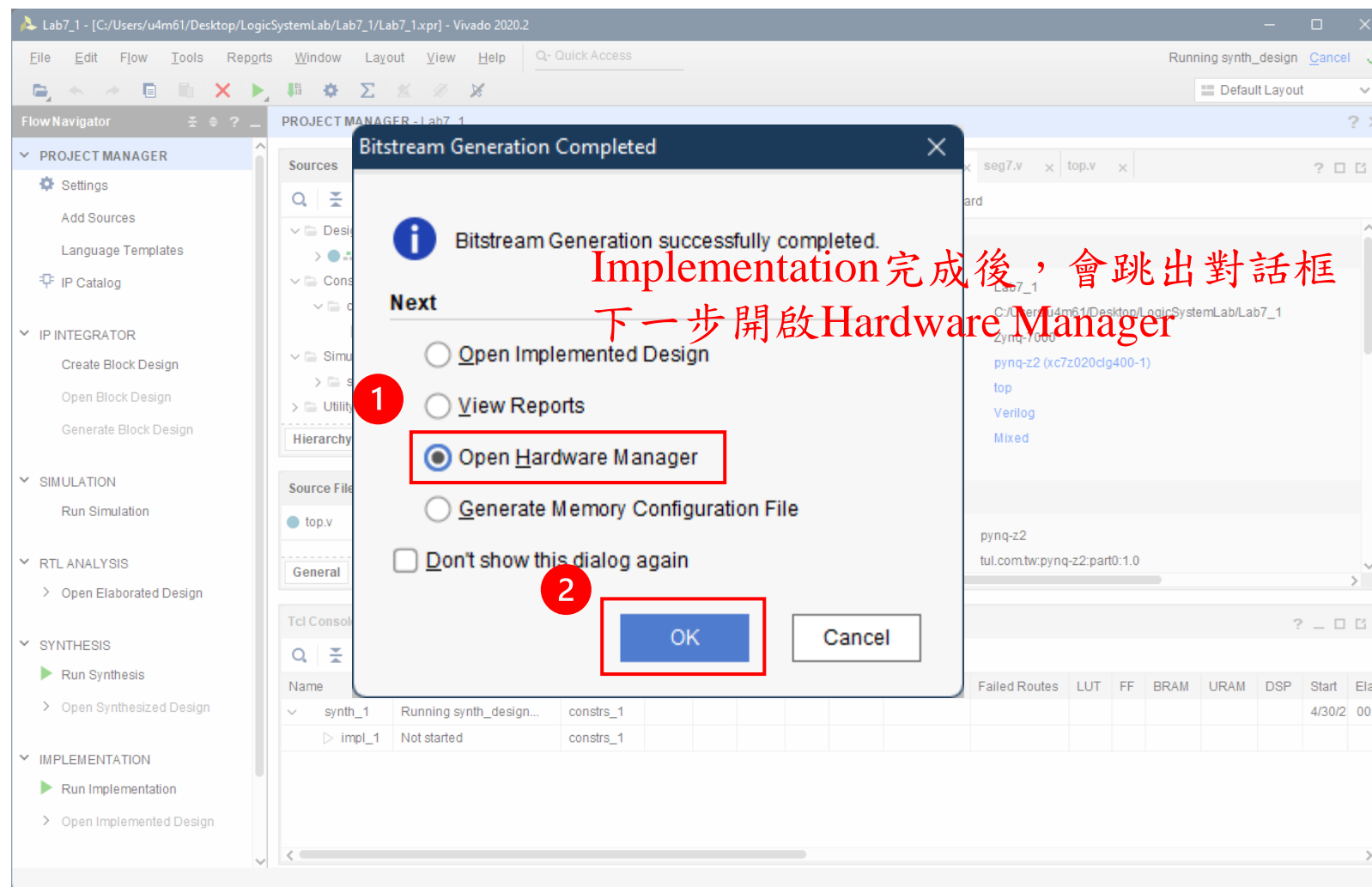


產生 Bitstream

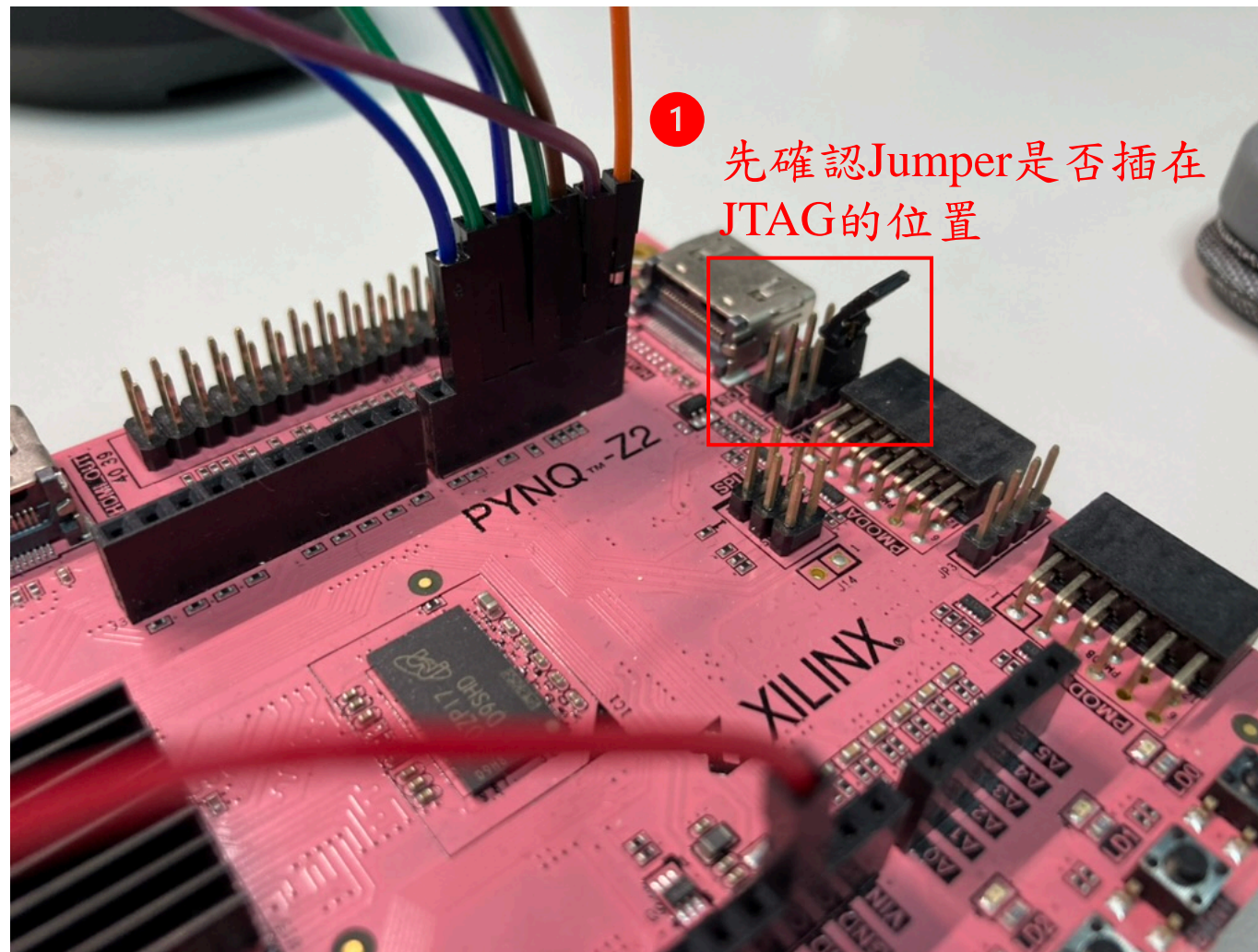
Implementation 完成後，會跳出對話框
下一步直接選擇 Generate Bitstream



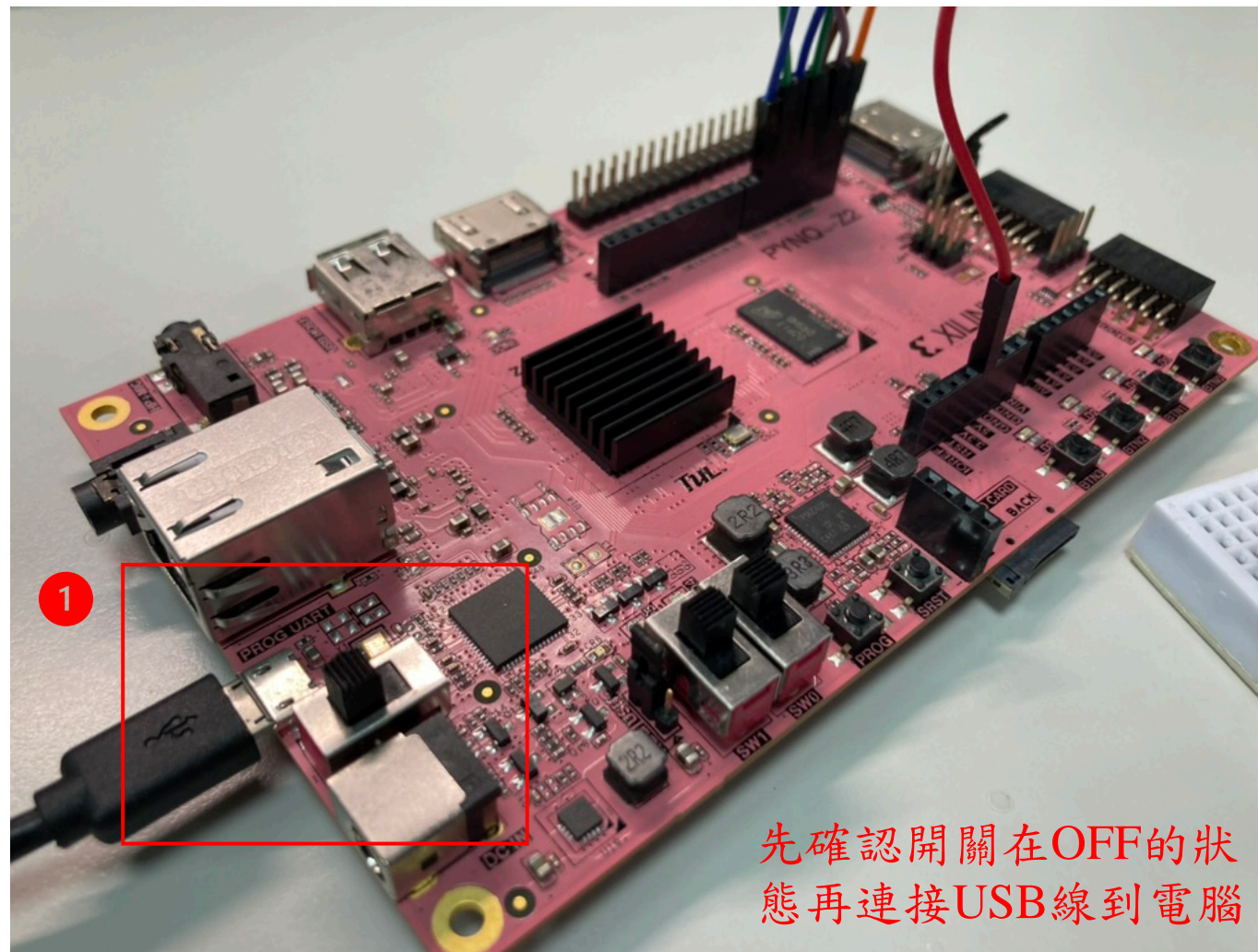
開啟Hardware Manager



連接PYNQ-Z2

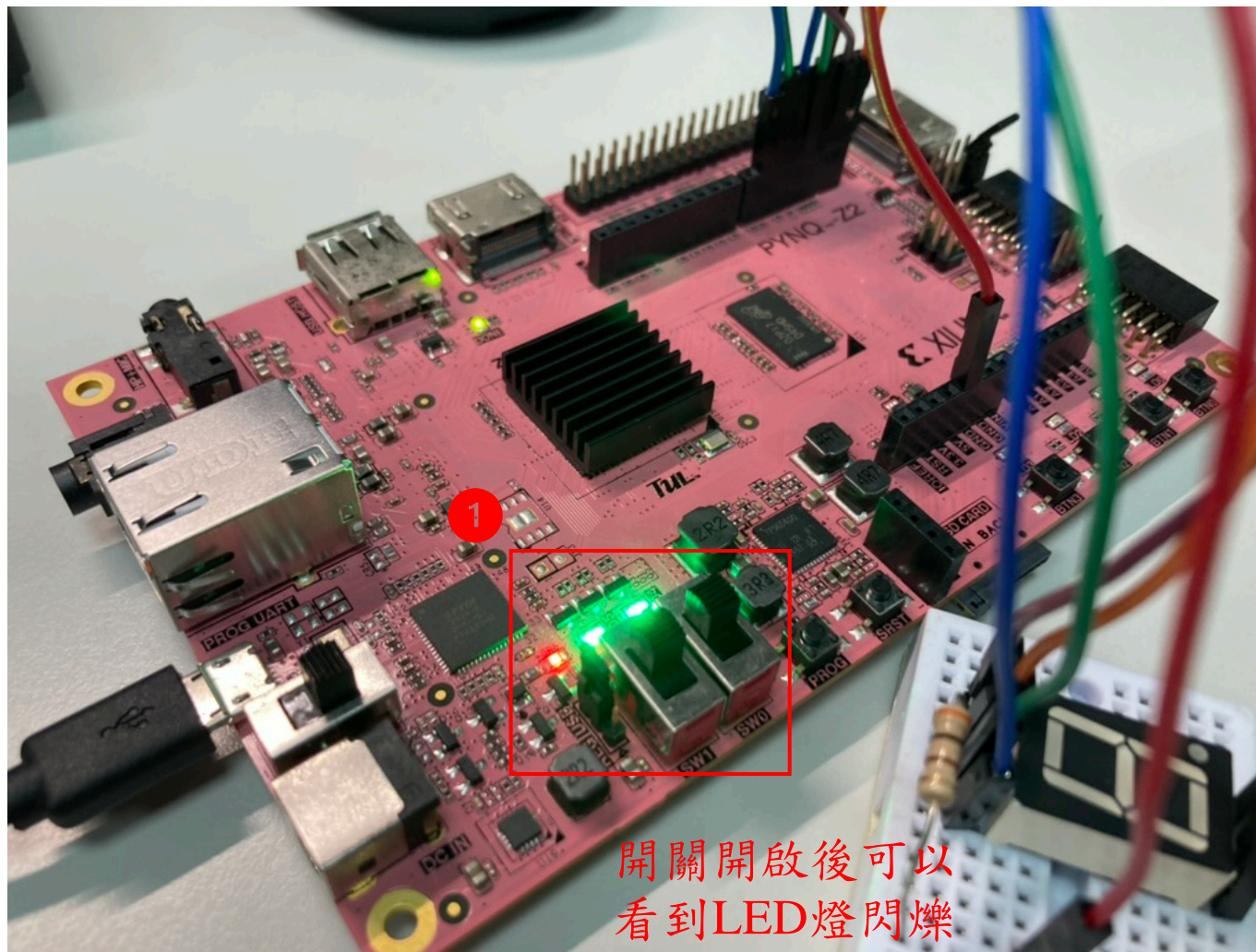


連接PYNQ-Z2

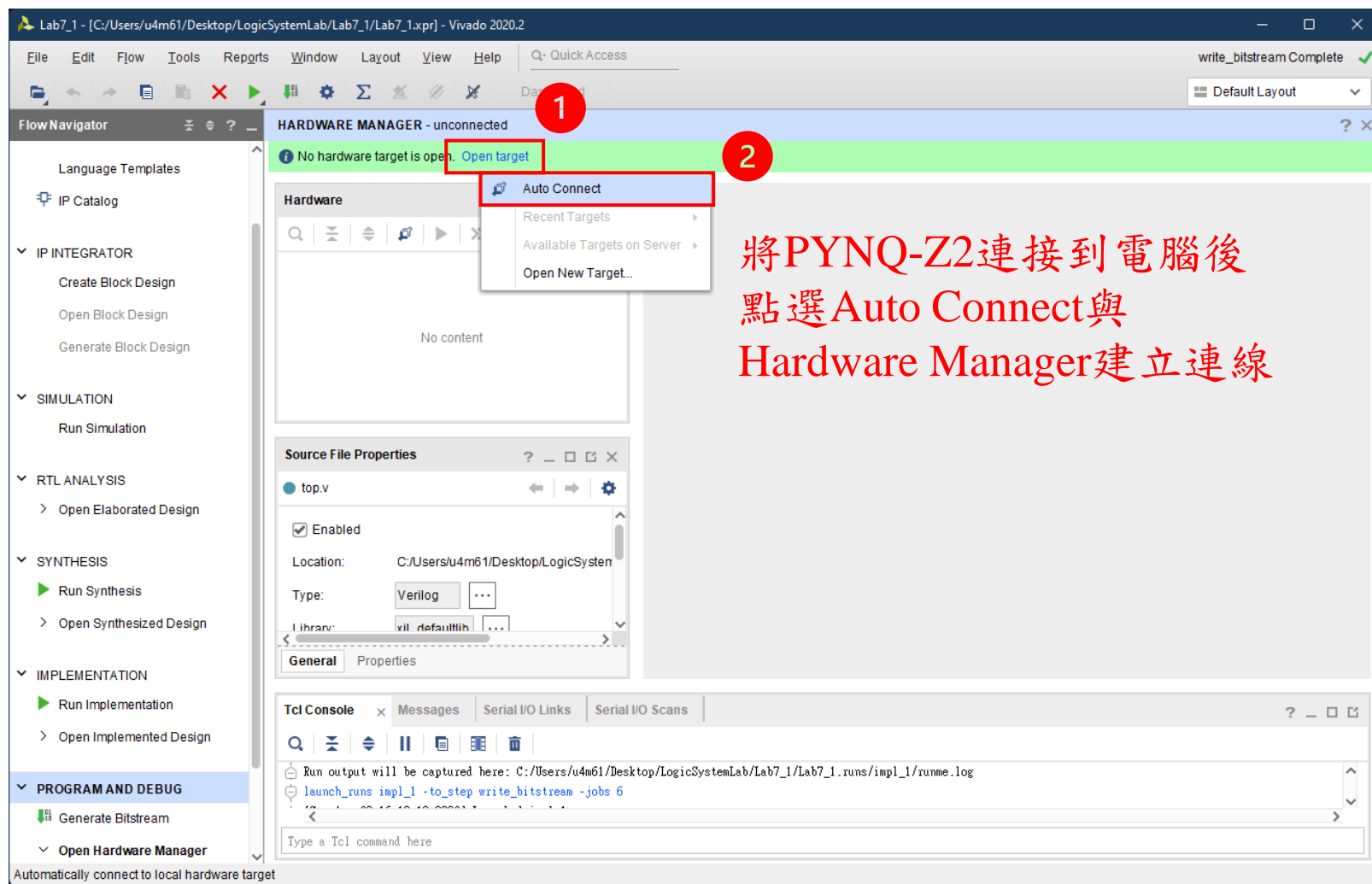


先確認開關在OFF的狀態再連接USB線到電腦

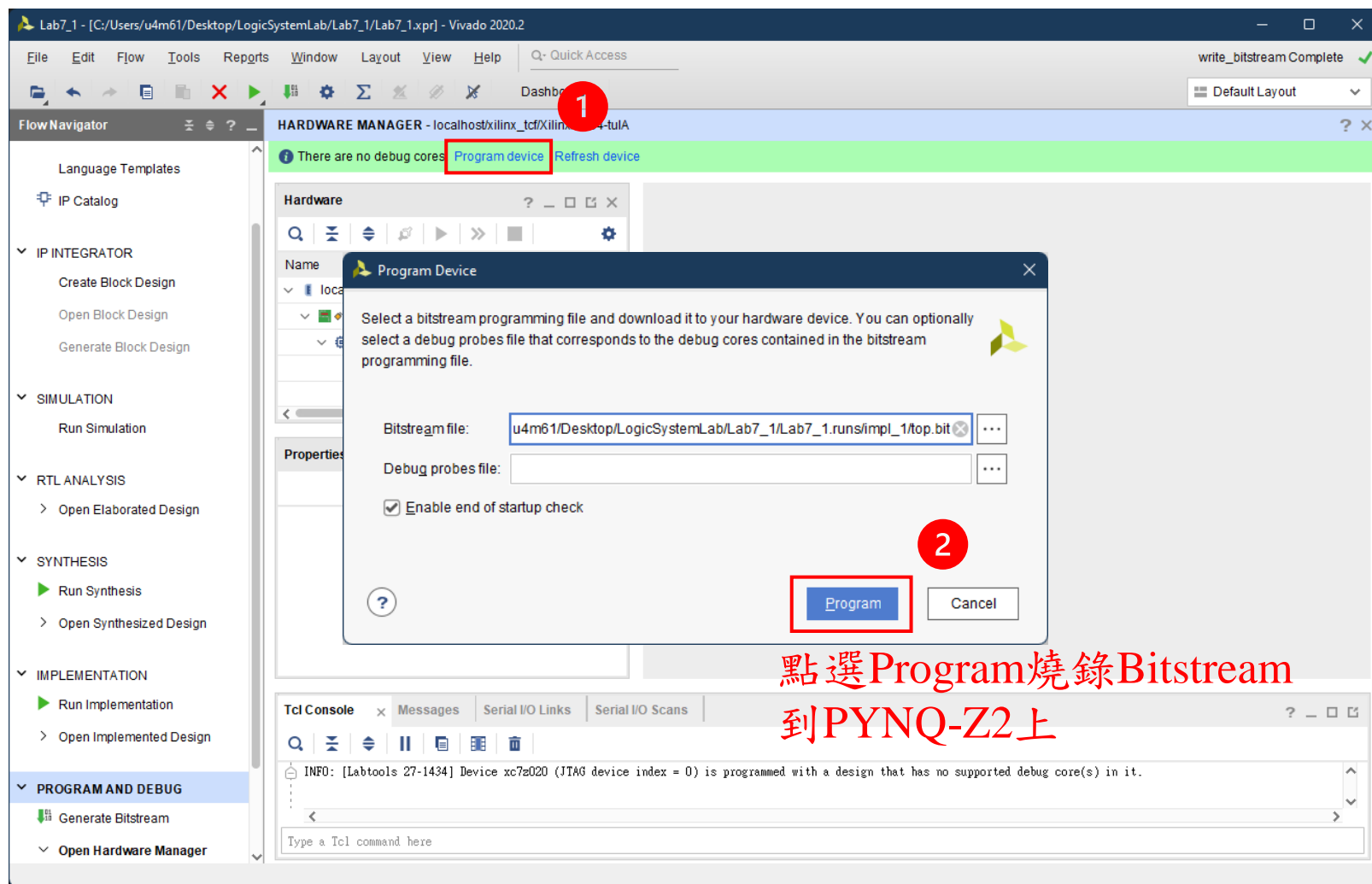
連接PYNQ-Z2



燒錄Bitstream到PYNQ-Z2上



燒錄Bitstream到PYNQ-Z2上



點選Program燒錄Bitstream
到PYNQ-Z2上

提示一

Lab7_1 - [C:/Users/u4m61/Desktop/LogicSystemLab/Lab7_1/Lab7_1.xpr] - Vivado 2020.2

File Edit Flow Tools Reports Window Layout View Help Q- Quick Access write_bitstream Complete ✓ Default Layout

Flow Navigator

- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream**
 - Open Hardware Manager
 - Open Target
 - Program Device
 - Add Configuration Memory Device

SYNTHESIZED DESIGN - xc7z020clg400-1

Sources x Netlist ? - □ □

- Design Sources (1)
 - top (top.v) (1)
- Constraints (1)
 - constrs_1 (1)
 - Lab7_1.xdc
- Simulation Sources (1)
 - sim_1 (1)
- Utility Sources

Hierarchy Libraries Comp4 ▶

Properties ? - □ □ □

Select an object to see properties

Project Summary x Device x Schematic x ? □ □

Overview | Dashboard

Settings Edit

Project name:	Lab7_1
Project location:	C:/Users/u4m61/Desktop/LogicSystemLab/Lab7_1
Product family:	Zynq-7000
Project part:	pynq-z2 (xc7z020clg400-1)
Top module name:	top
Target language:	Verilog
Simulator language:	Mixed

Board Part

Display name:	pynq-z2
Board part name:	tul.com.tw:pynq-z2:part0:1.0
Board revision:	1.0
Connectors:	No connections

Tcl Console x Messages Log Reports Design Runs ? - □ □

Finished Parsing XDC File [C:/Users/u4m61/Desktop/LogicSystemLab/Lab7_1/constrs/Lab7_1.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 3011.055 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Type a Tcl command here

Generate a programming file after implementation

修改 Verilog 後必須重新跑過

1. Synthesis

2. Implementation

3. 以及 Generate Bitstream

直接按 Generate Bitstream 會

幫你重新跑過所有流程

提示二

Lab7_1 - [C:/Users/u4m61/Desktop/LogicSystemLab/Lab7_1/Lab7_1.xpr] - Vivado 2020.2

File Edit Flow Tools Reports Window Layout View Help Q- Quick Access write_bitstream Complete

Flow Navigator

- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Set Up Debug
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic**
- IMPLEMENTATION
 - Run Implementation

SYNTHESIZED DESIGN - xc7z020clg400-1

Sources Netlist

- top
 - Nets (22)
 - Leaf Cells (11)
 - i_seg7 (seg7)

Properties

Select an object to see properties

Project Summary Device Schematic

12 Cells 11 I/O Ports 22 Nets

btn[3:0] i_seg7 ar[6:0]

btn_IBUF[0]_inst IBUF btn_IBUF[1]_inst IBUF btn_IBUF[2]_inst IBUF btn_IBUF[3]_inst IBUF

seg7

ar_OBUF[0]_inst OBUF ar_OBUF[1]_inst OBUF ar_OBUF[2]_inst OBUF ar_OBUF[3]_inst OBUF ar_OBUF[4]_inst OBUF ar_OBUF[5]_inst OBUF ar_OBUF[6]_inst OBUF

Tcl Console Messages Log Reports Design Runs

Finished Parsing XDC File [C:/Users/u4m61/Desktop/LogicSystemLab/Lab7_1/constr/Lab7_1.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 3011.055 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Type a Tcl command here

點選Open Synthesized Design
底下的Schematic可以顯示合
成後的邏輯電路圖，確認
Module是否有正確連接