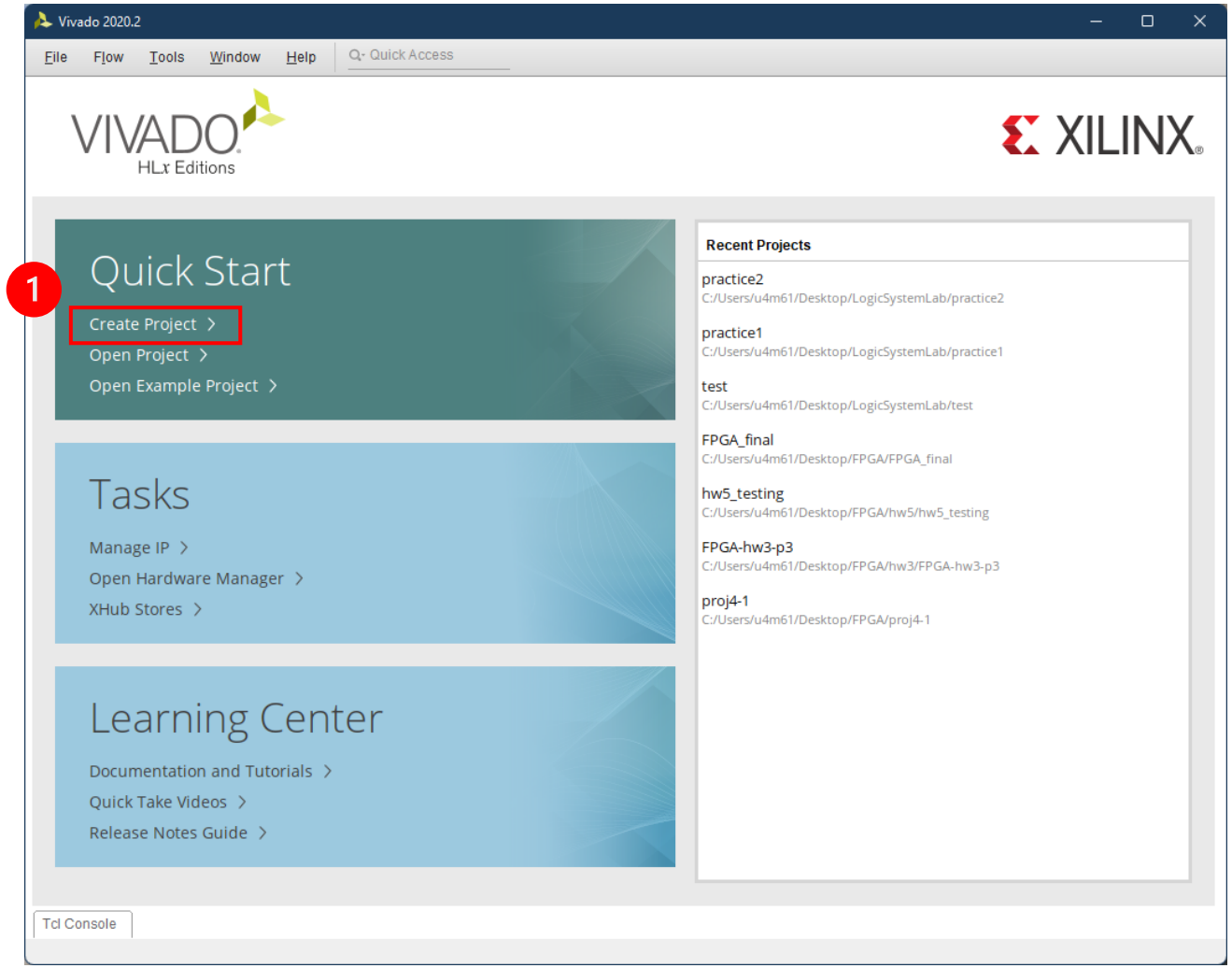
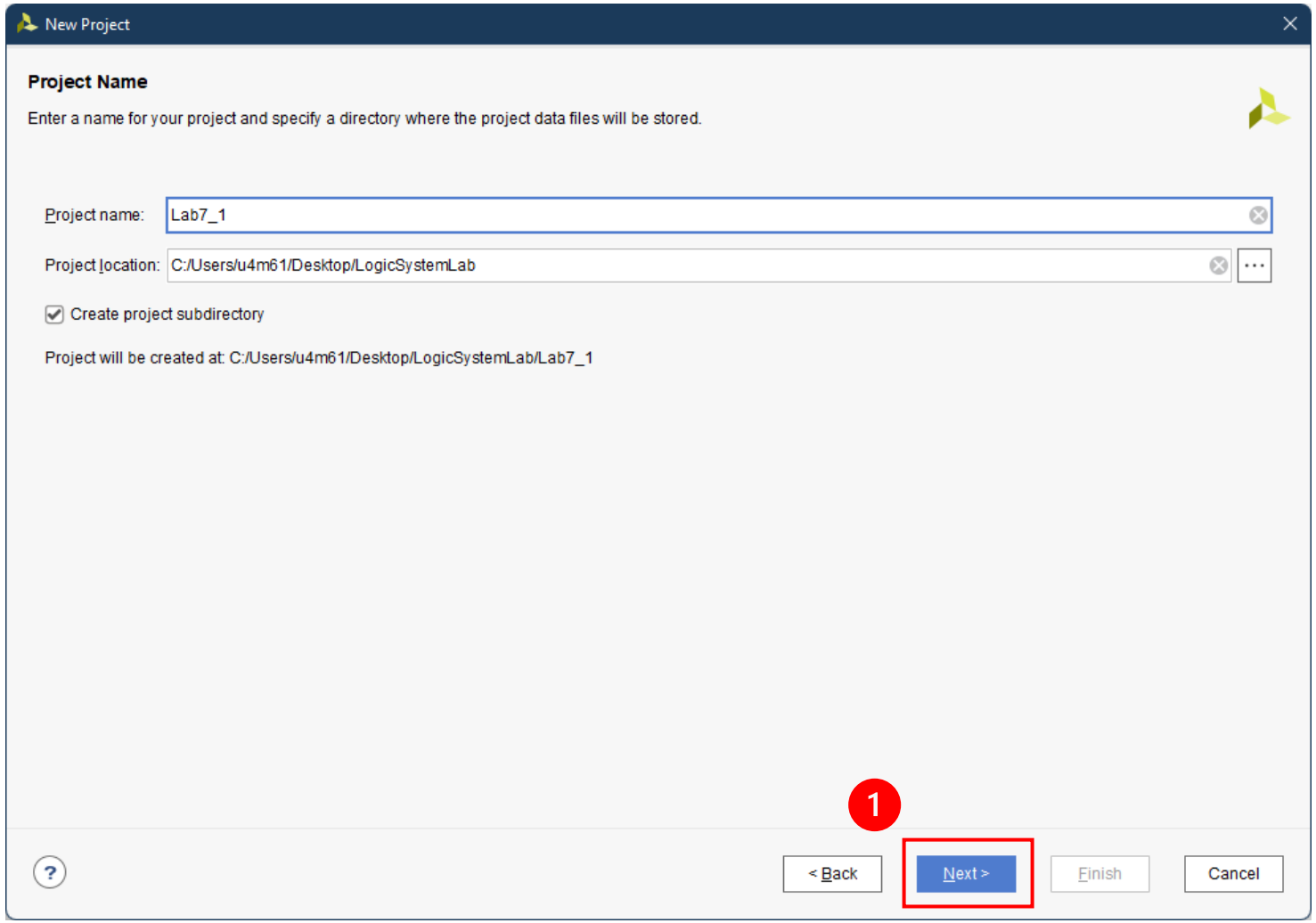
Laboratory 7
PYNQ操作教學

Department of Electrical Engineering
National Cheng Kung University

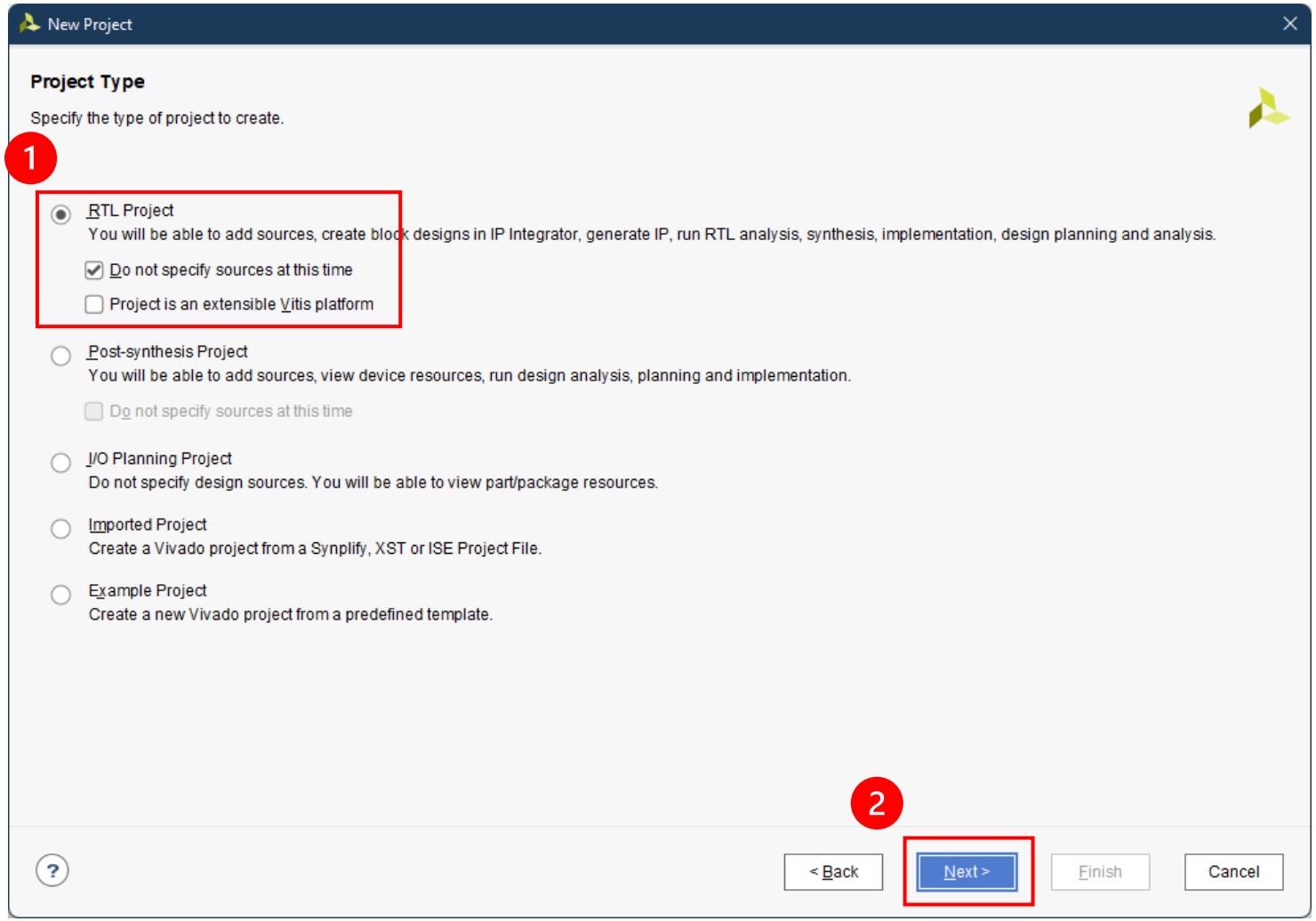
新增Project


Vivado 2020.2
File
Flow
Tools
Window
Help
Quick Access
VIVADO
HLx Editions
XILINX
1
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
XHub Stores
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
Recent Projects
practice2
C:/Users/u4m61/Desktop/LogicSystemLab/practice2
practice1
C:/Users/u4m61/Desktop/LogicSystemLab/practice1
test
C:/Users/u4m61/Desktop/LogicSystemLab/test
FPGA_final
C:/Users/u4m61/Desktop/FPGA/FPGA_final
hw5_testing
C:/Users/u4m61/Desktop/FPGA/hw5/hw5_testing
FPGA-hw3-p3
C:/Users/u4m61/Desktop/FPGA/hw3/FPGA-hw3-p3
proj4-1
C:/Users/u4m61/Desktop/FPGA/proj4-1
Tcl Console

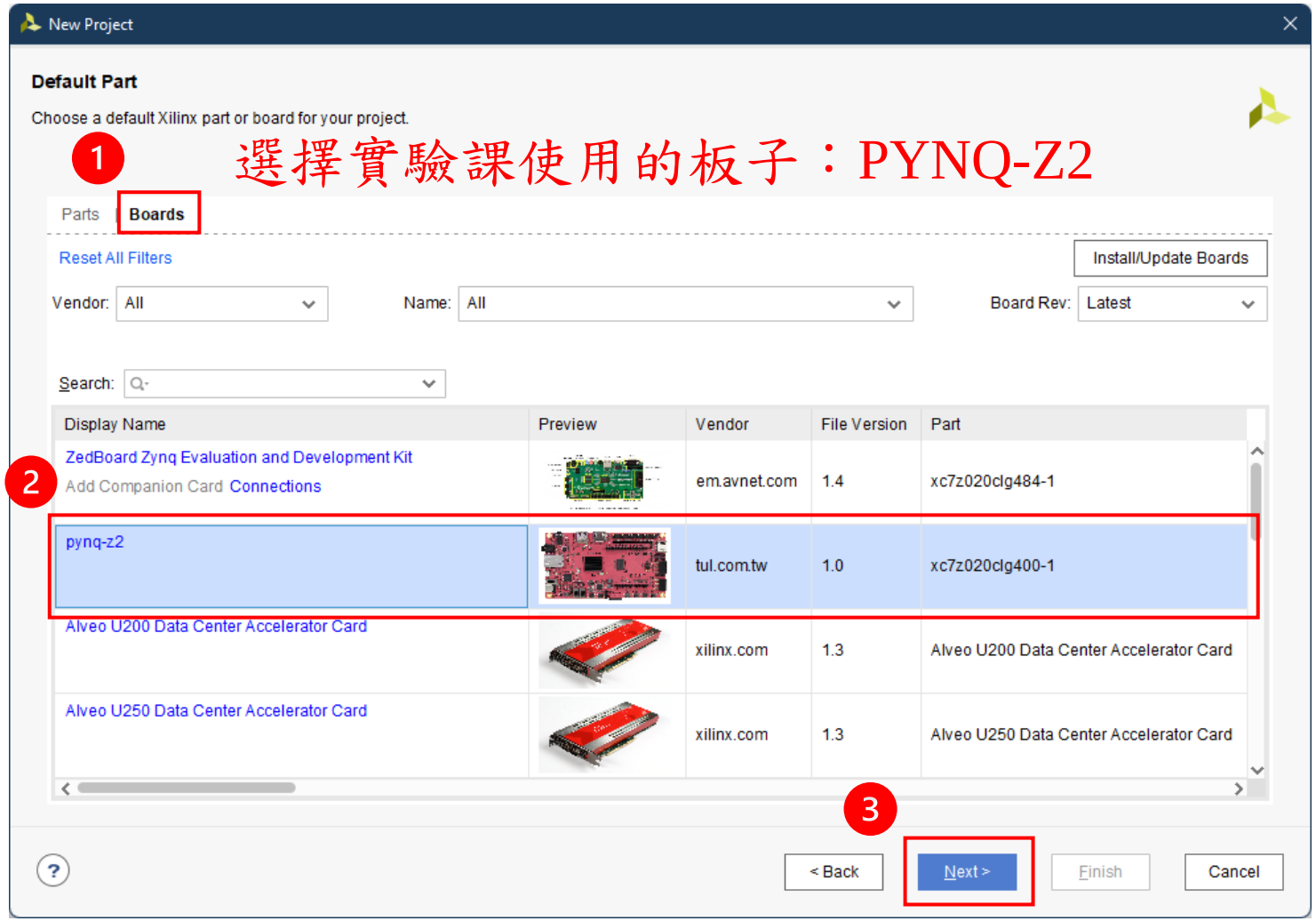
新增Project


New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
Lab7_1
Project location:
C:/Users/u4m61/Desktop/LogicSystemLab
Create project subdirectory
Project will be created at: C:/Users/u4m61/Desktop/LogicSystemLab/Lab7_1
1
< Back
Next >
Finish
Cancel

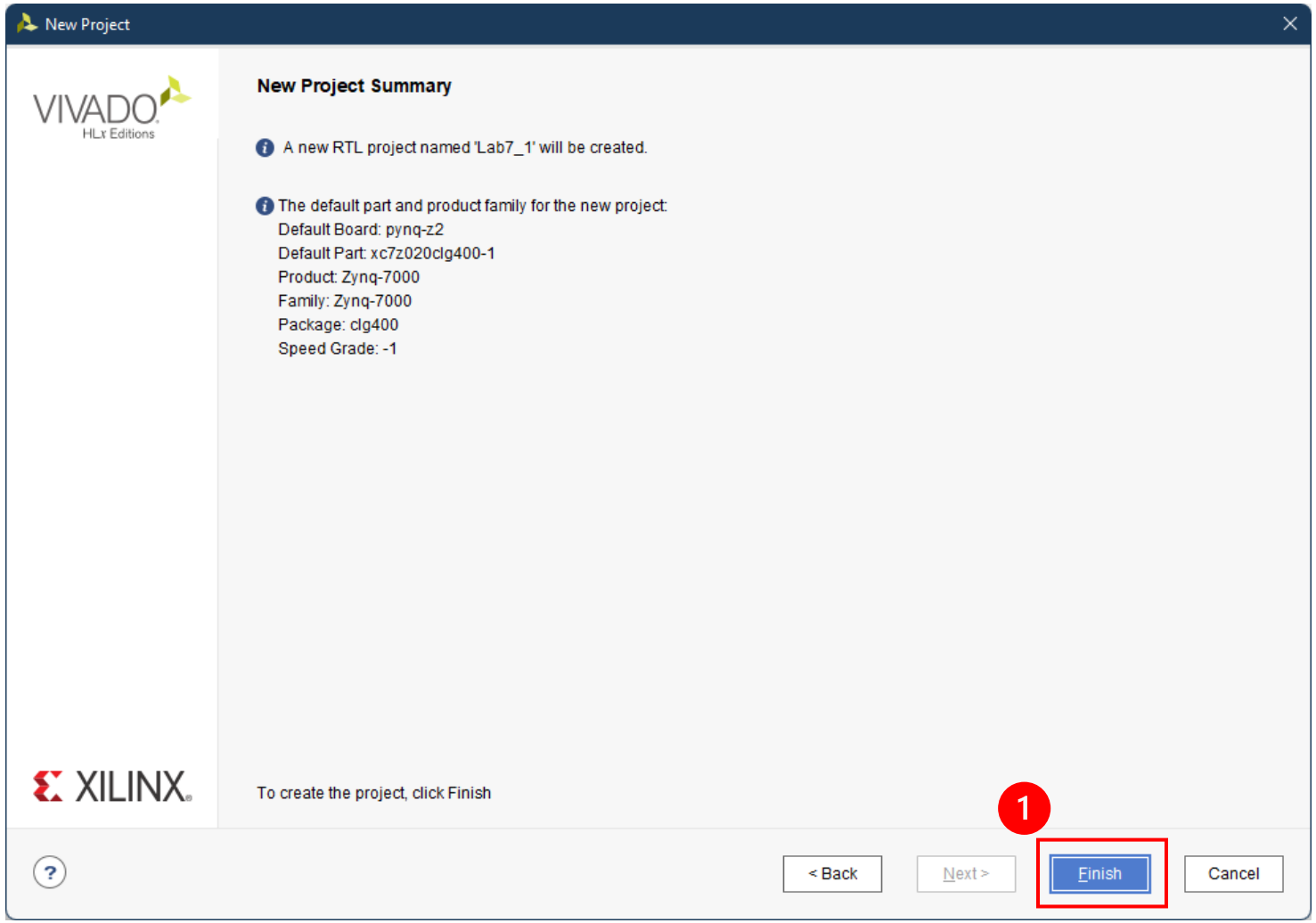
新增Project


New Project
Project Type
Specify the type of project to create.
1
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
2
< Back
Next >
Finish
Cancel

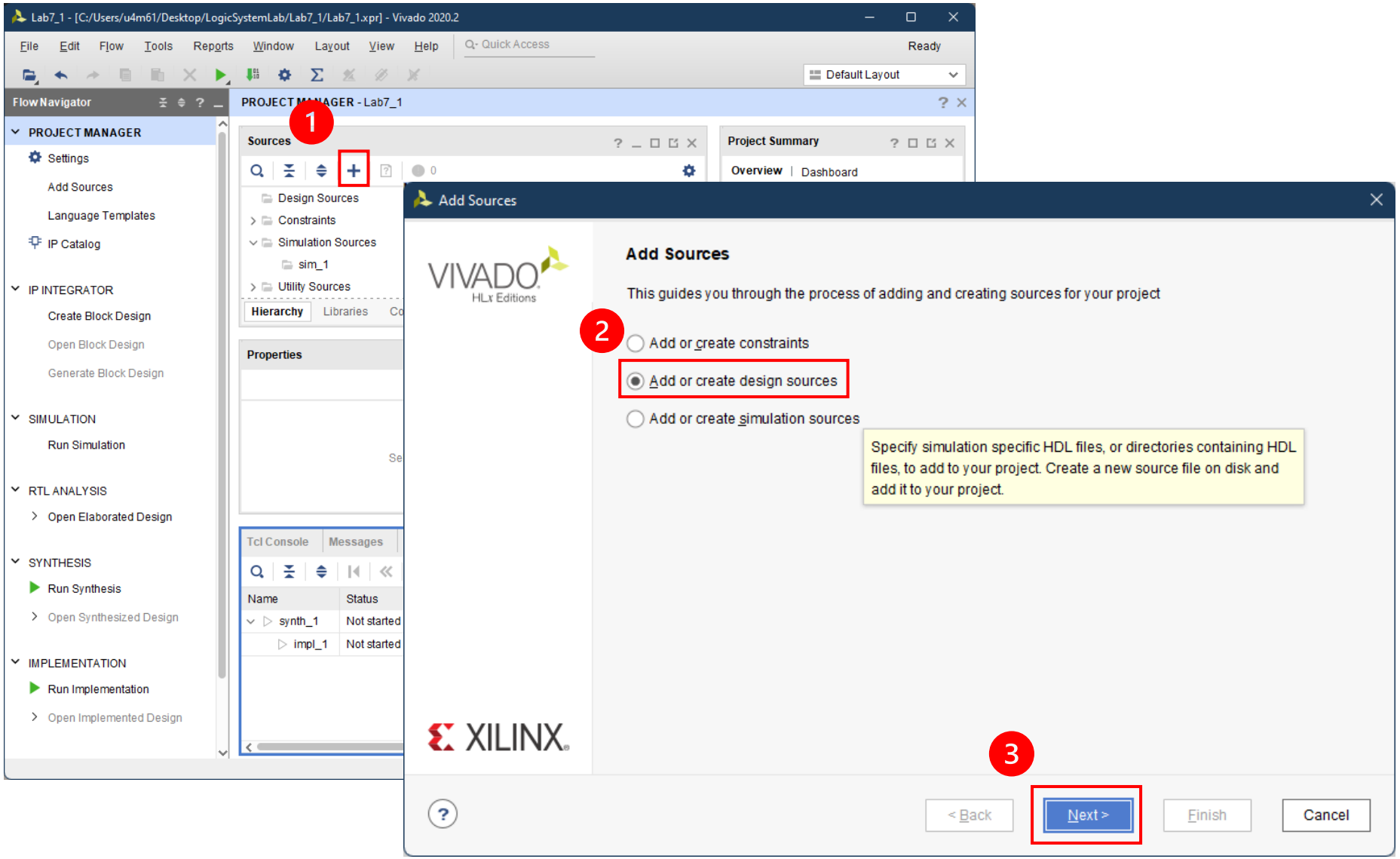
新增Project


New Project
Default Part
Choose a default Xilinx part or board for your project.
1
選擇實驗課使用的板子：PYNQ-Z2
Parts
Boards
Reset All Filters
Install/Update Boards
Vendor: All
Name: All
Board Rev: Latest
Search:
Display Name
Preview
Vendor
File Version
Part
ZedBoard Zynq Evaluation and Development Kit
Add Companion Card Connections
em.avnet.com
1.4
xc7z020clg484-1
2
pynq-z2
tul.com.tw
1.0
xc7z020clg400-1
Alveo U200 Data Center Accelerator Card
xilinx.com
1.3
Alveo U200 Data Center Accelerator Card
Alveo U250 Data Center Accelerator Card
xilinx.com
1.3
Alveo U250 Data Center Accelerator Card
3
< Back
Next >
Finish
Cancel

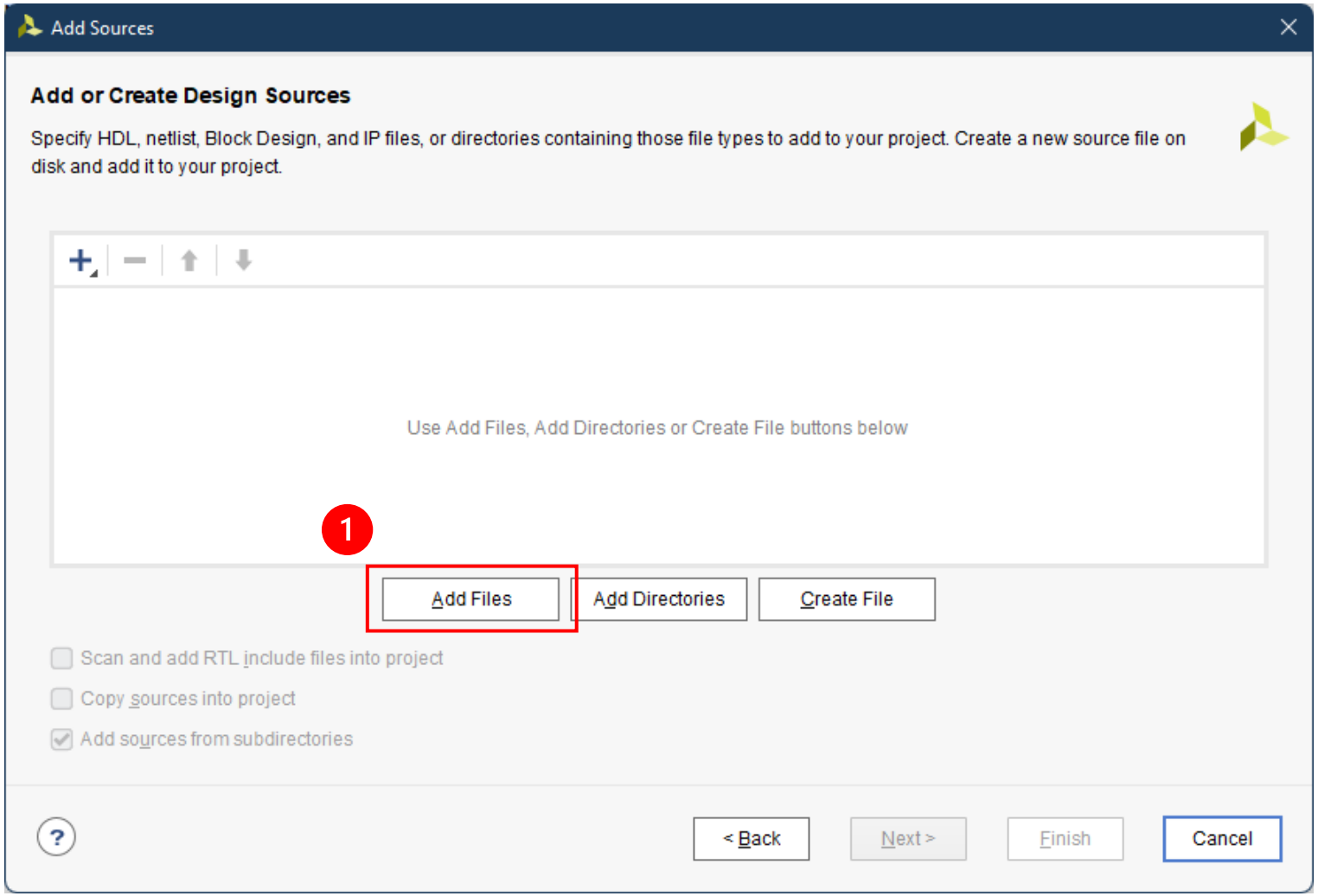
新增Project


New Project
VIVADO
HLx Editions
New Project Summary
A new RTL project named 'Lab7_1' will be created.
The default part and product family for the new project:
Default Board: pynq-z2
Default Part: xc7z020clg400-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg400
Speed Grade: -1
XILINX
To create the project, click Finish
1
< Back
Next >
Finish
Cancel

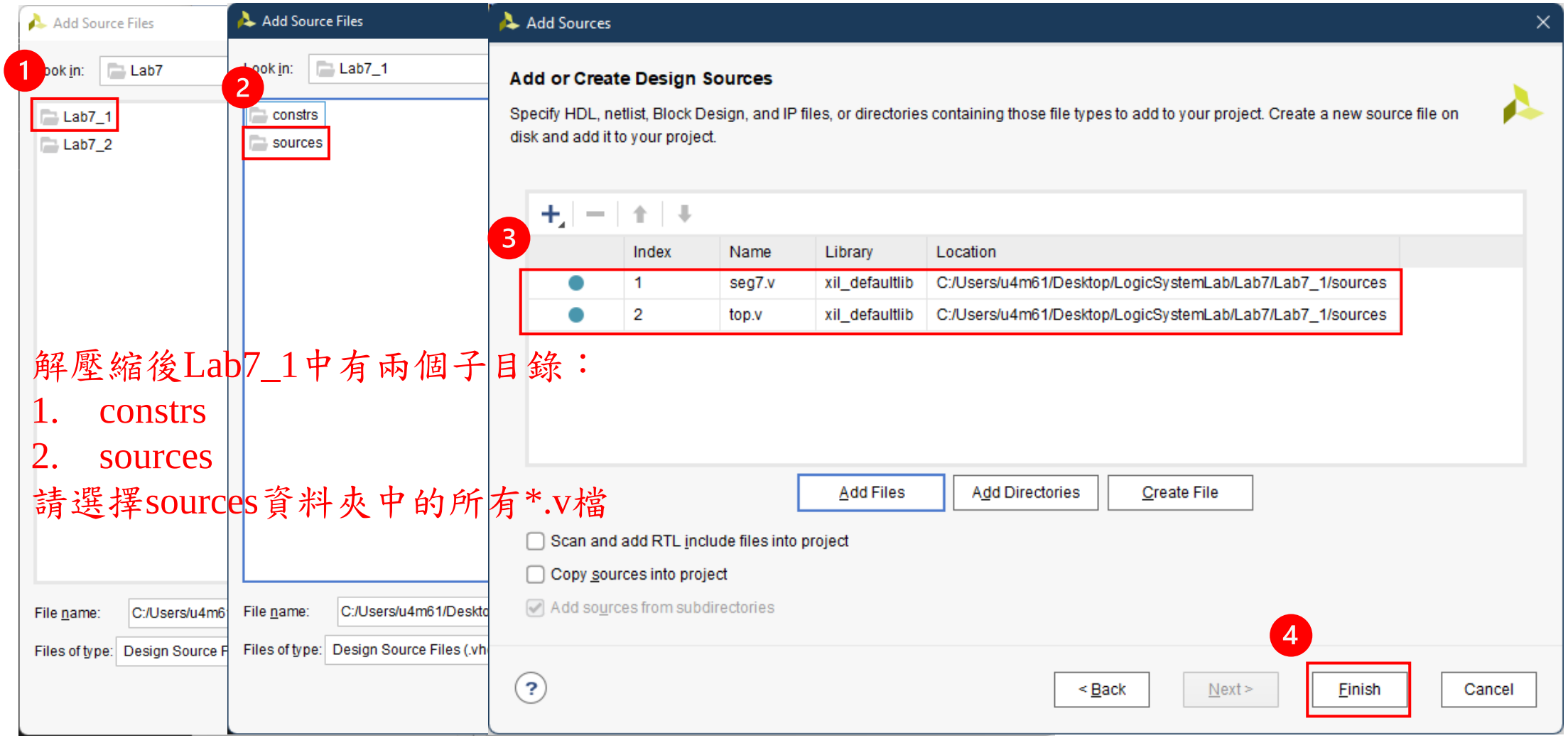
加入Verilog Source



加入Verilog Source



加入Verilog Source

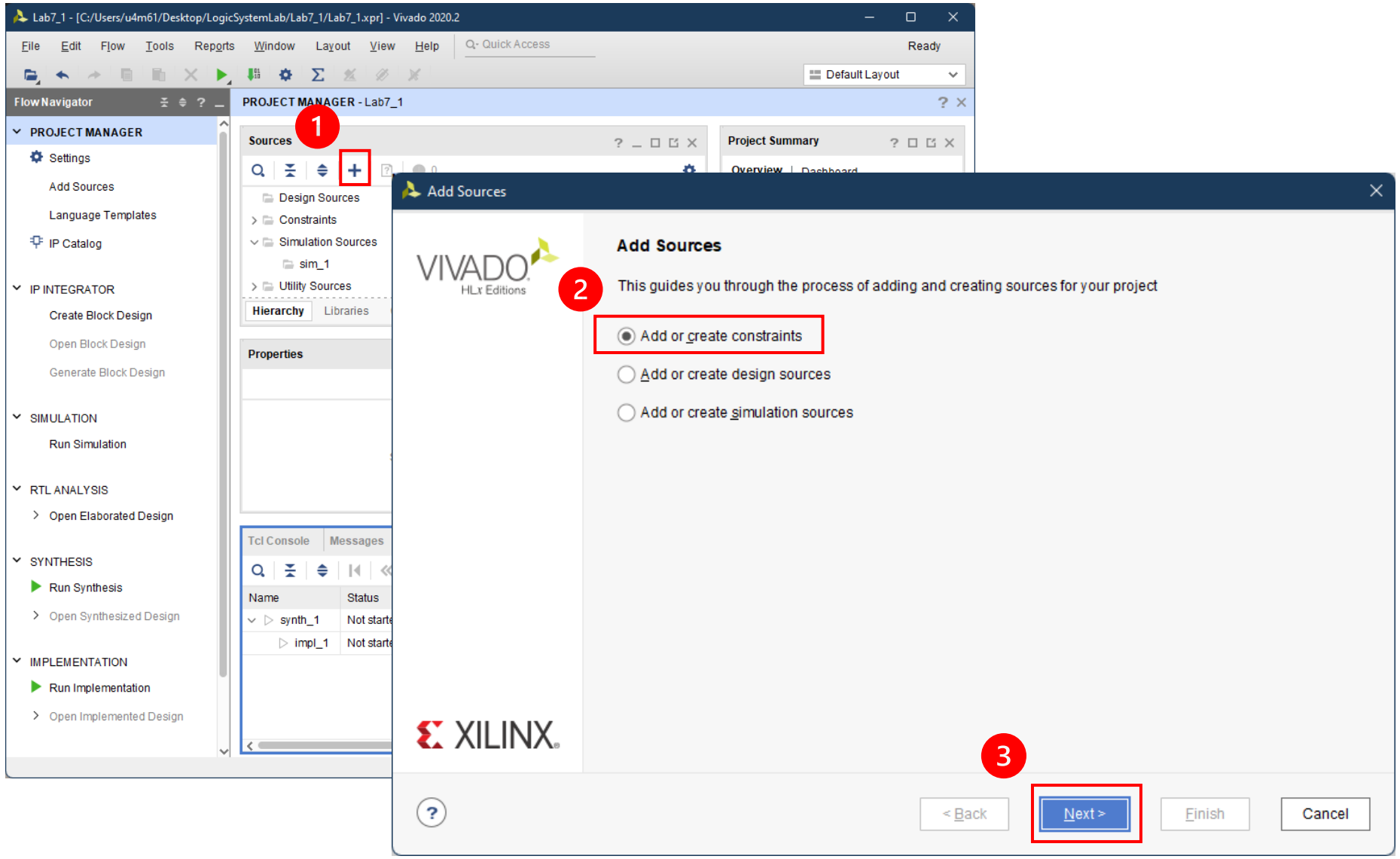


解壓縮後Lab7_1中有兩個子目錄：

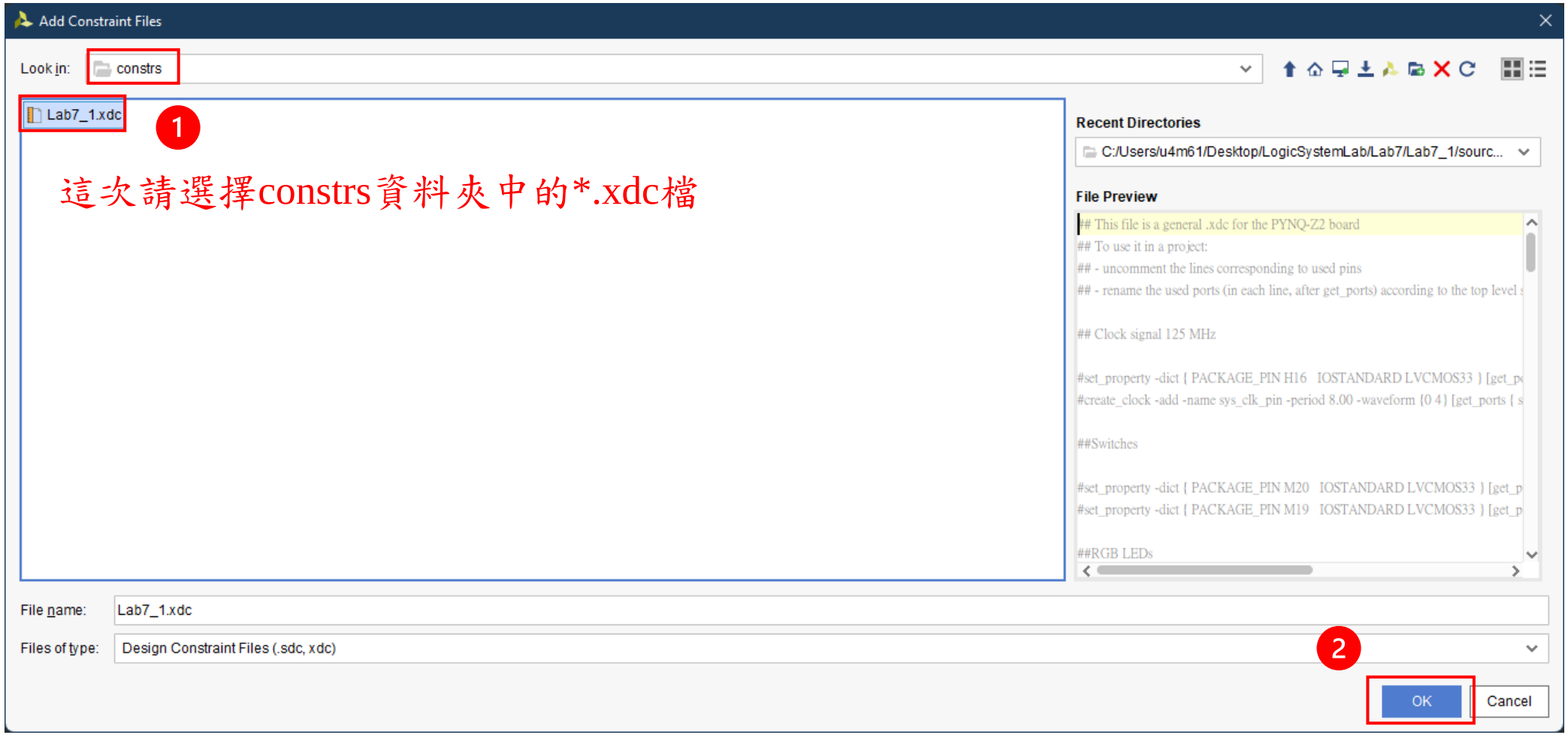
1. constrs
2. sources

請選擇sources資料夾中的所有*.v檔

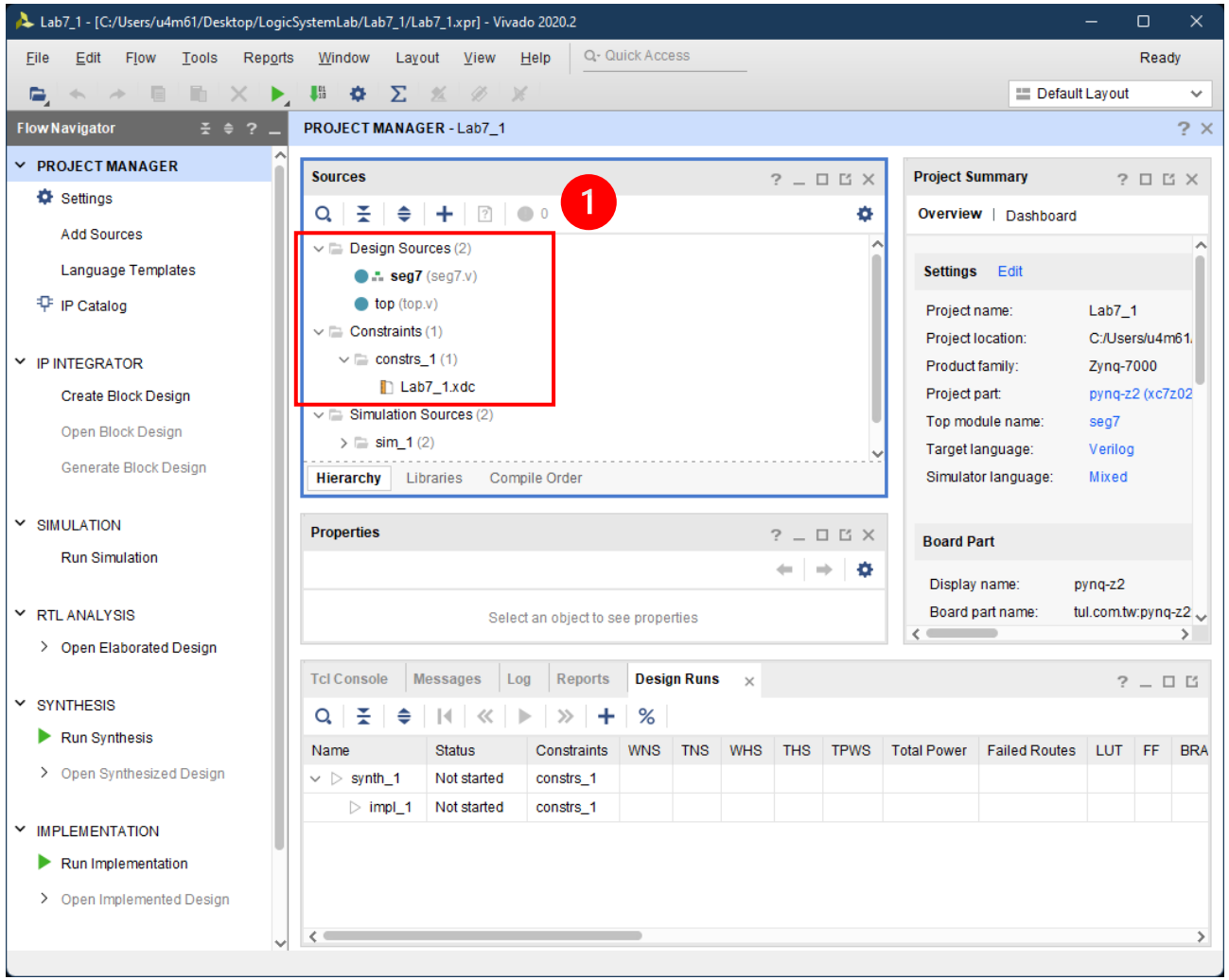
加入PYNQ Constraint



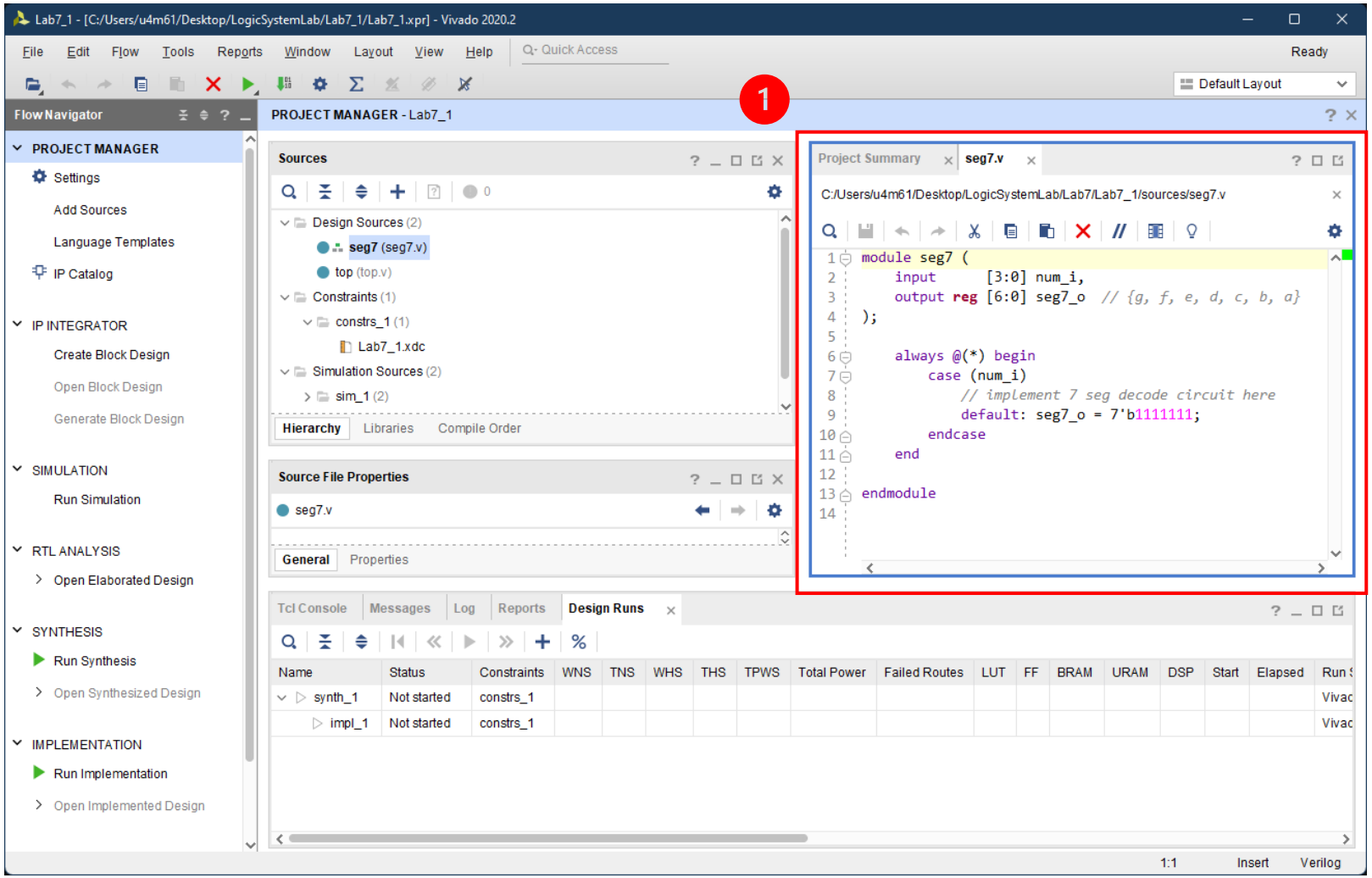
加入PYNQ Constraint



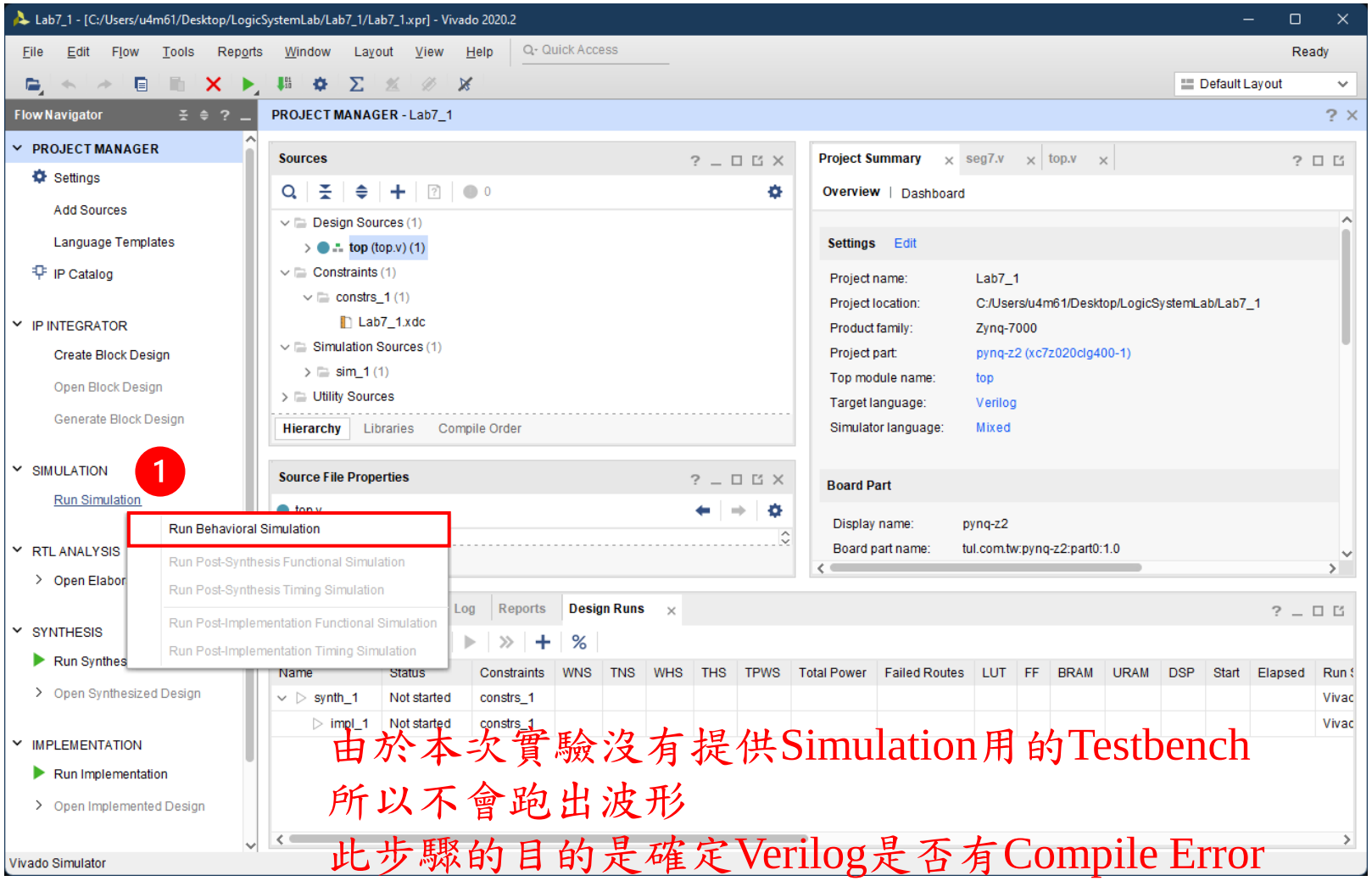
確定檔案成功加入Project



編輯Verilog檔案

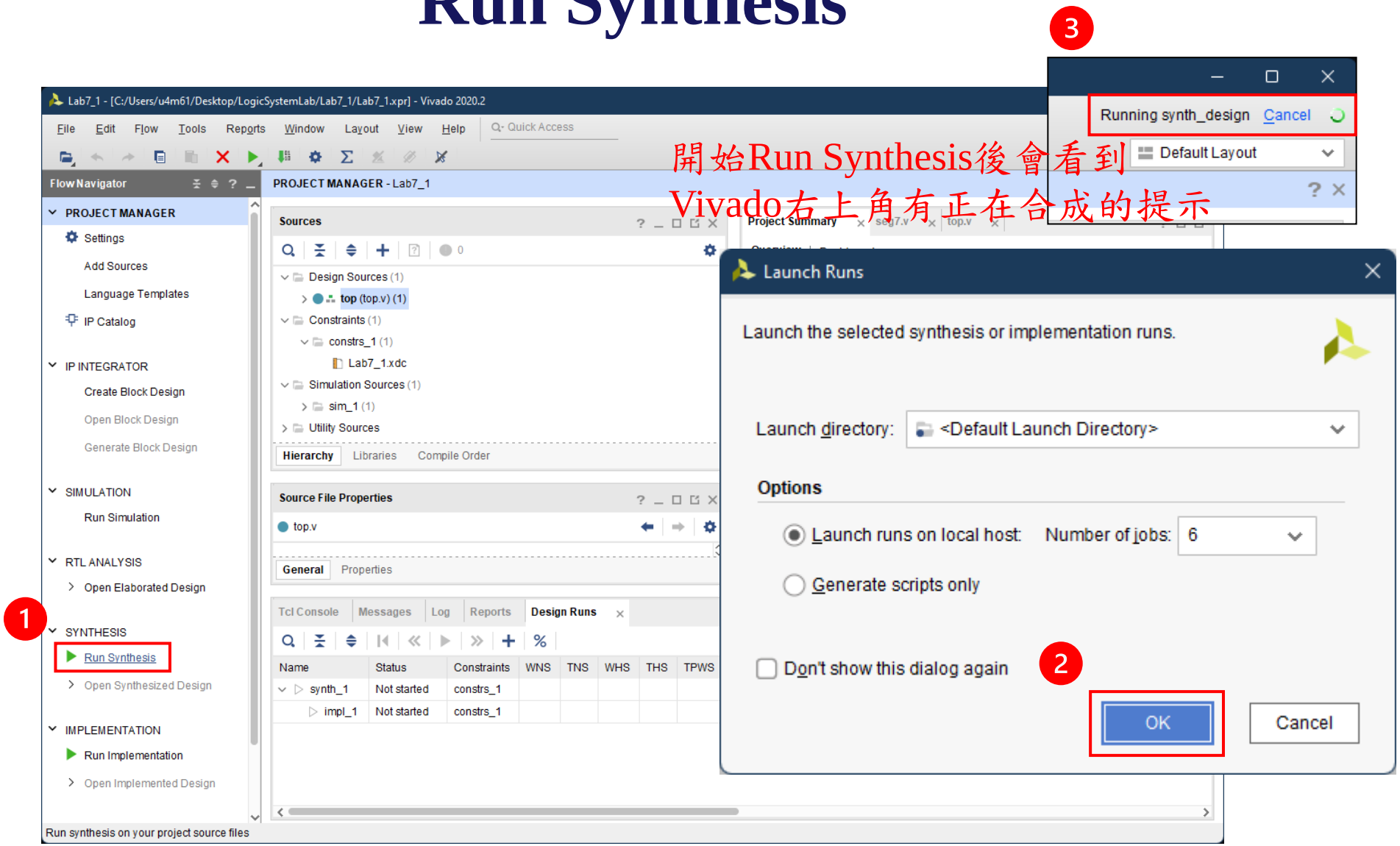


可以先Run Simulation確認有無錯誤



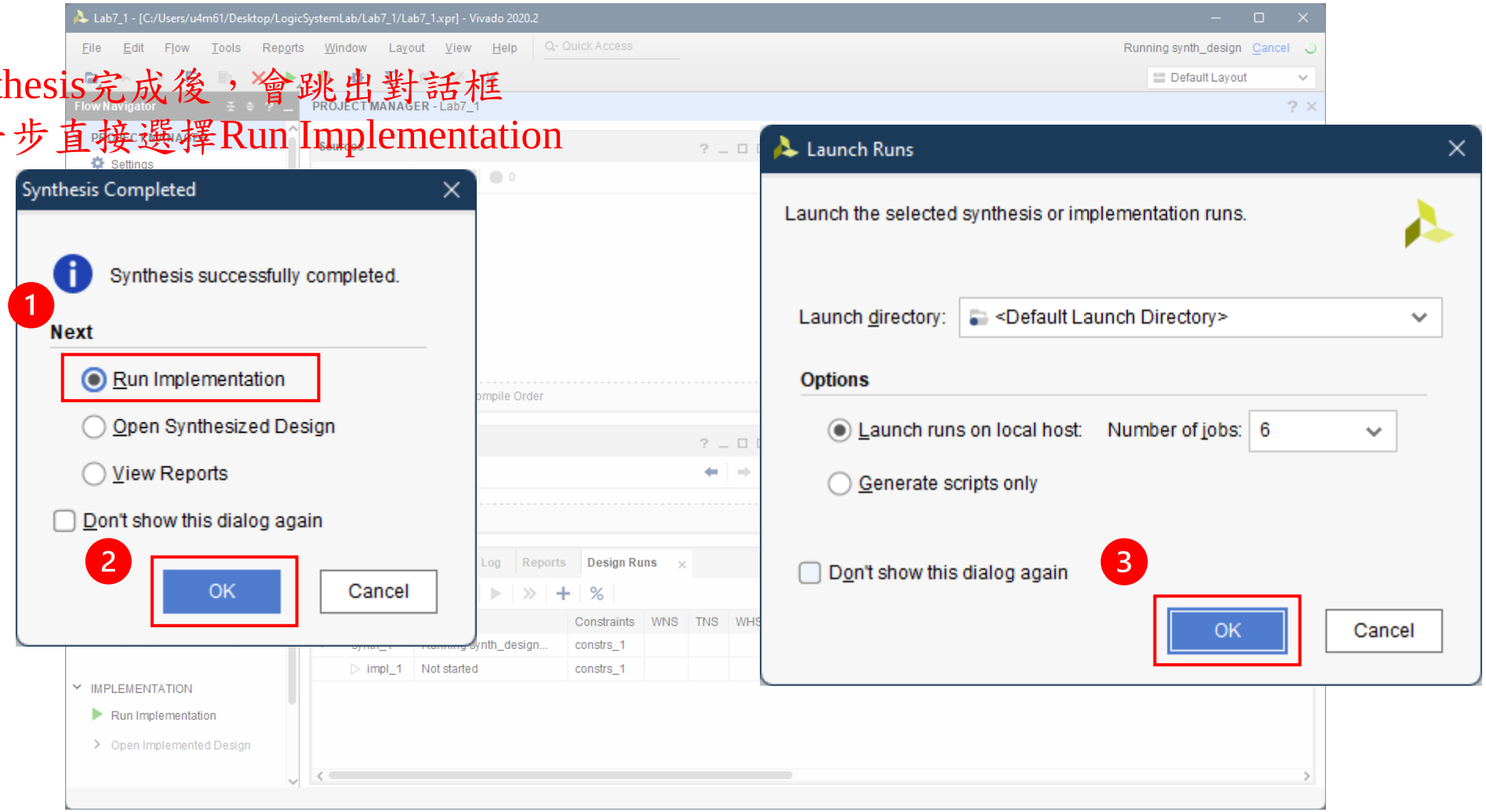
由於本次實驗沒有提供Simulation用的Testbench
所以不會跑出波形
此步驟的目的是確定Verilog是否有Compile Error

Run Synthesis



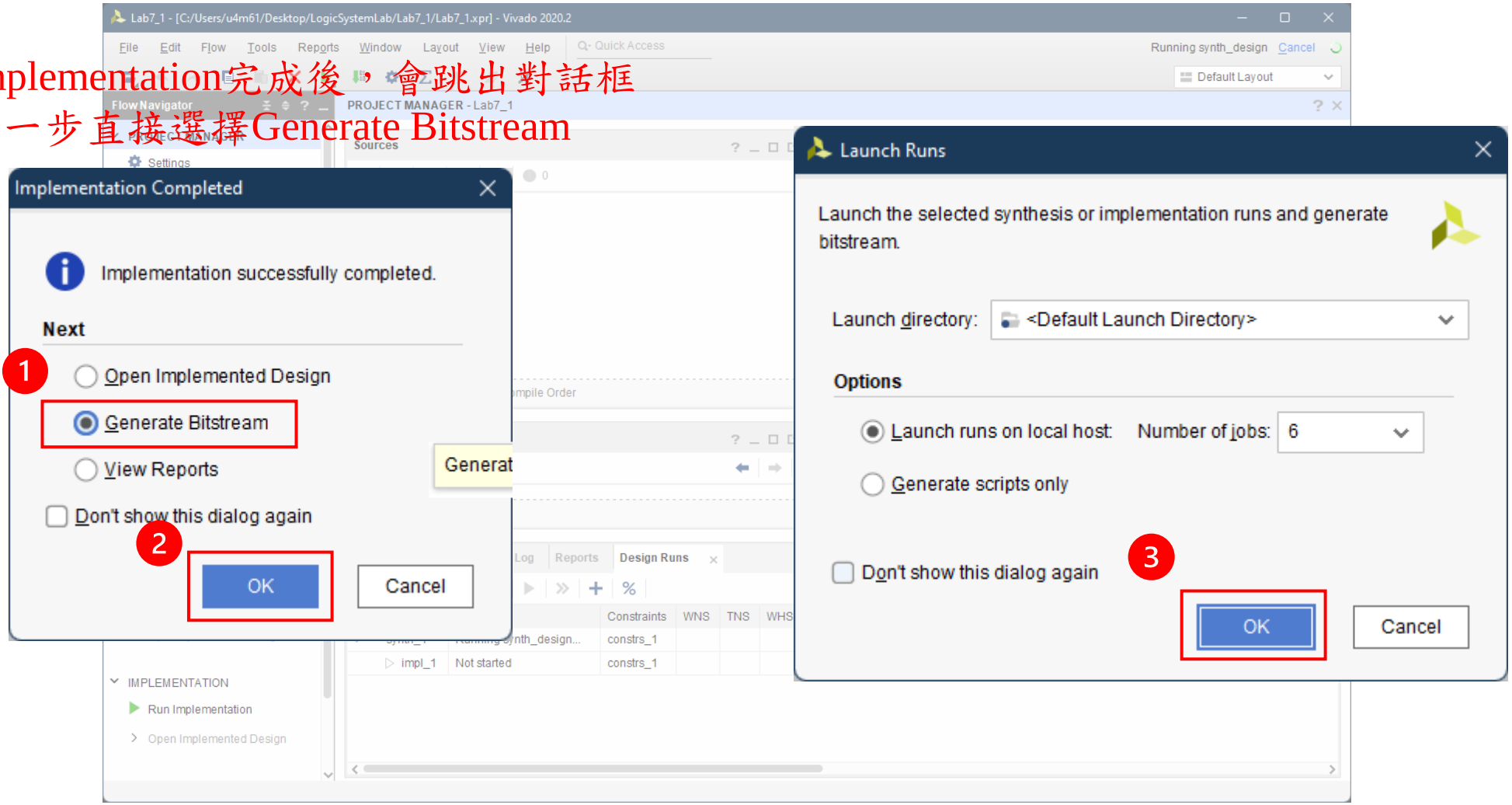
Run Implementation

Synthesis完成後，會跳出對話框
下一步直接選擇Run Implementation

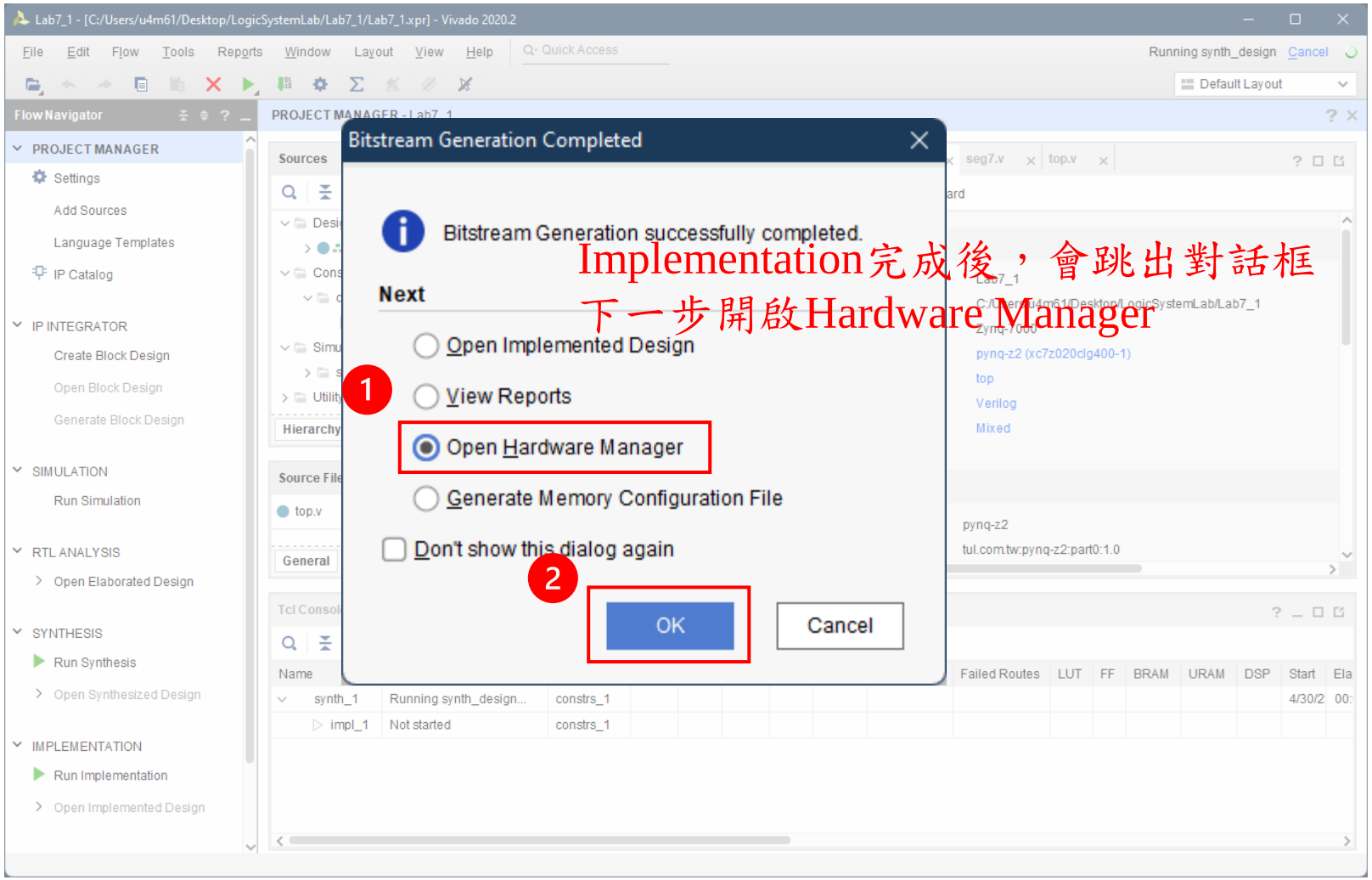


產生Bitstream

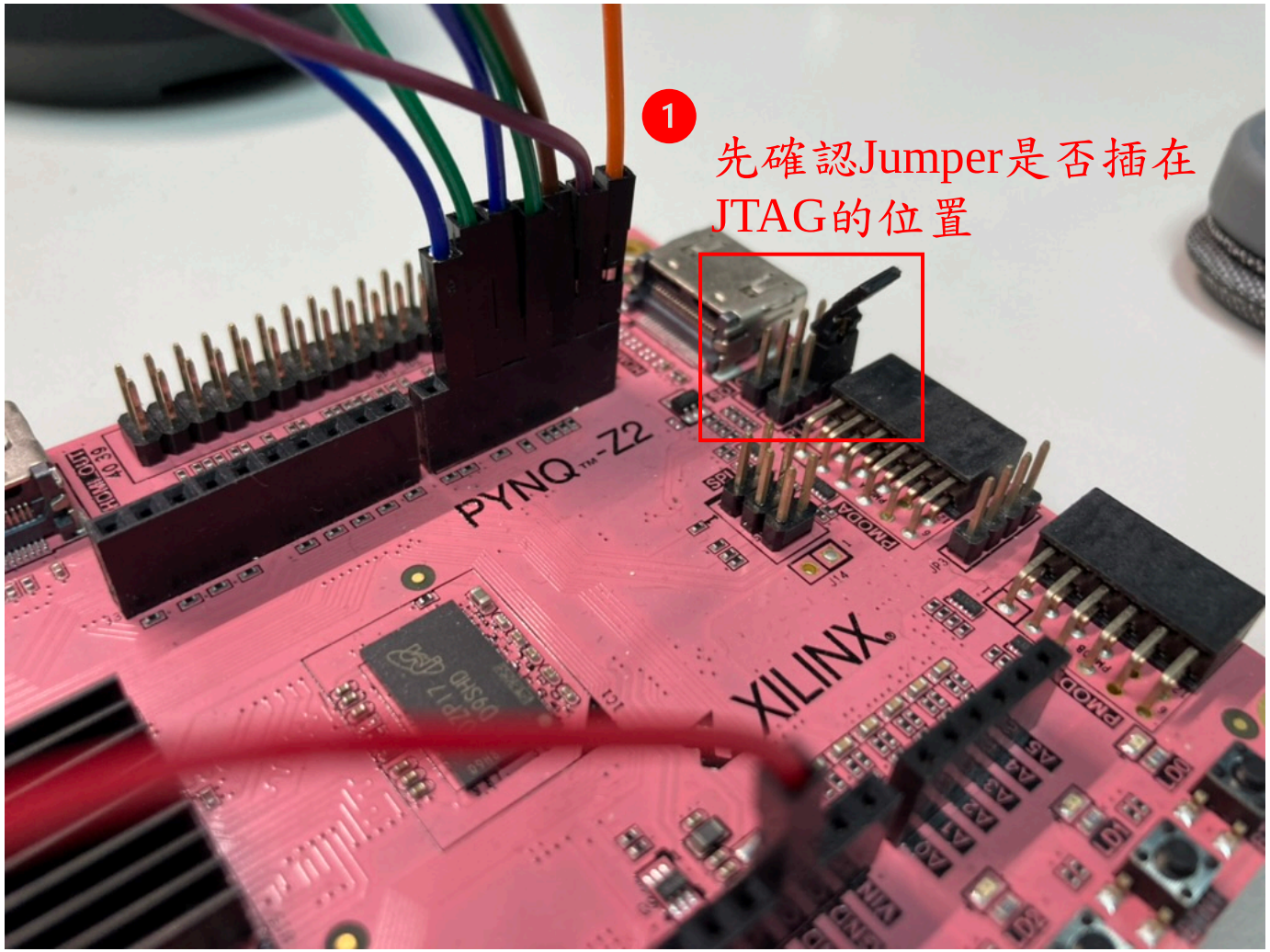
Implementation完成後，會跳出對話框
下一步直接選擇Generate Bitstream



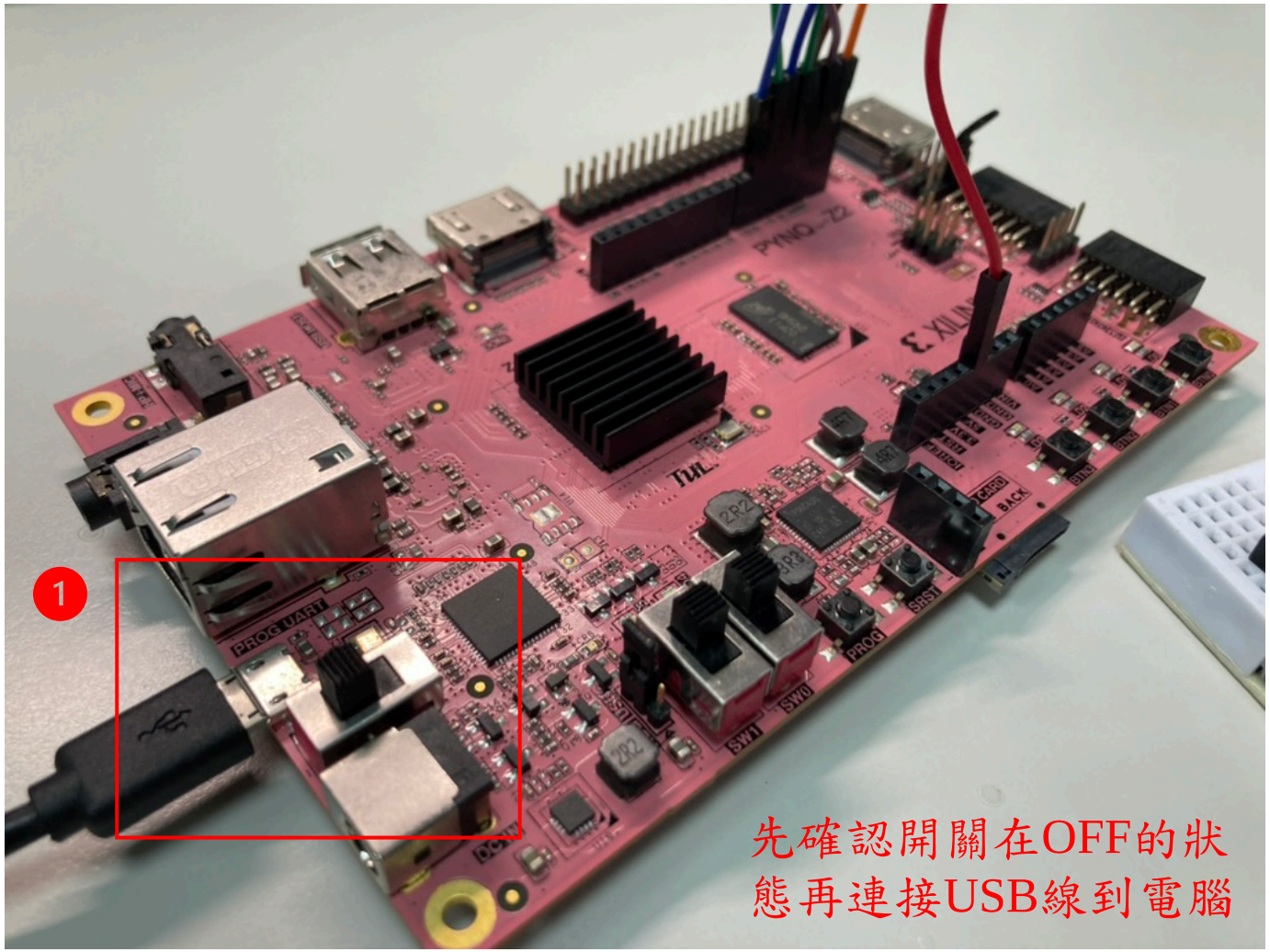
開啟Hardware Manager



連接PYNQ-Z2

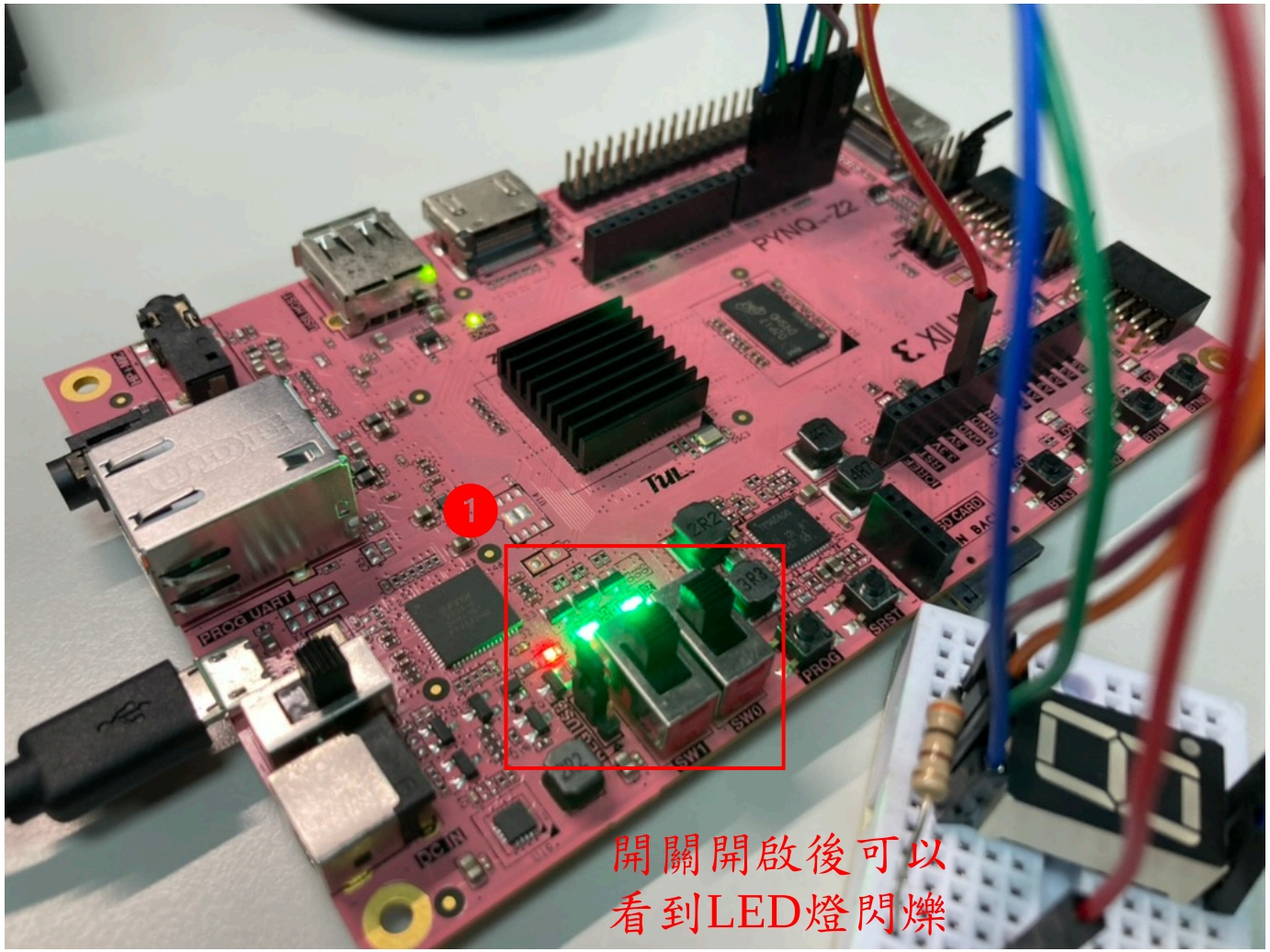


連接PYNQ-Z2

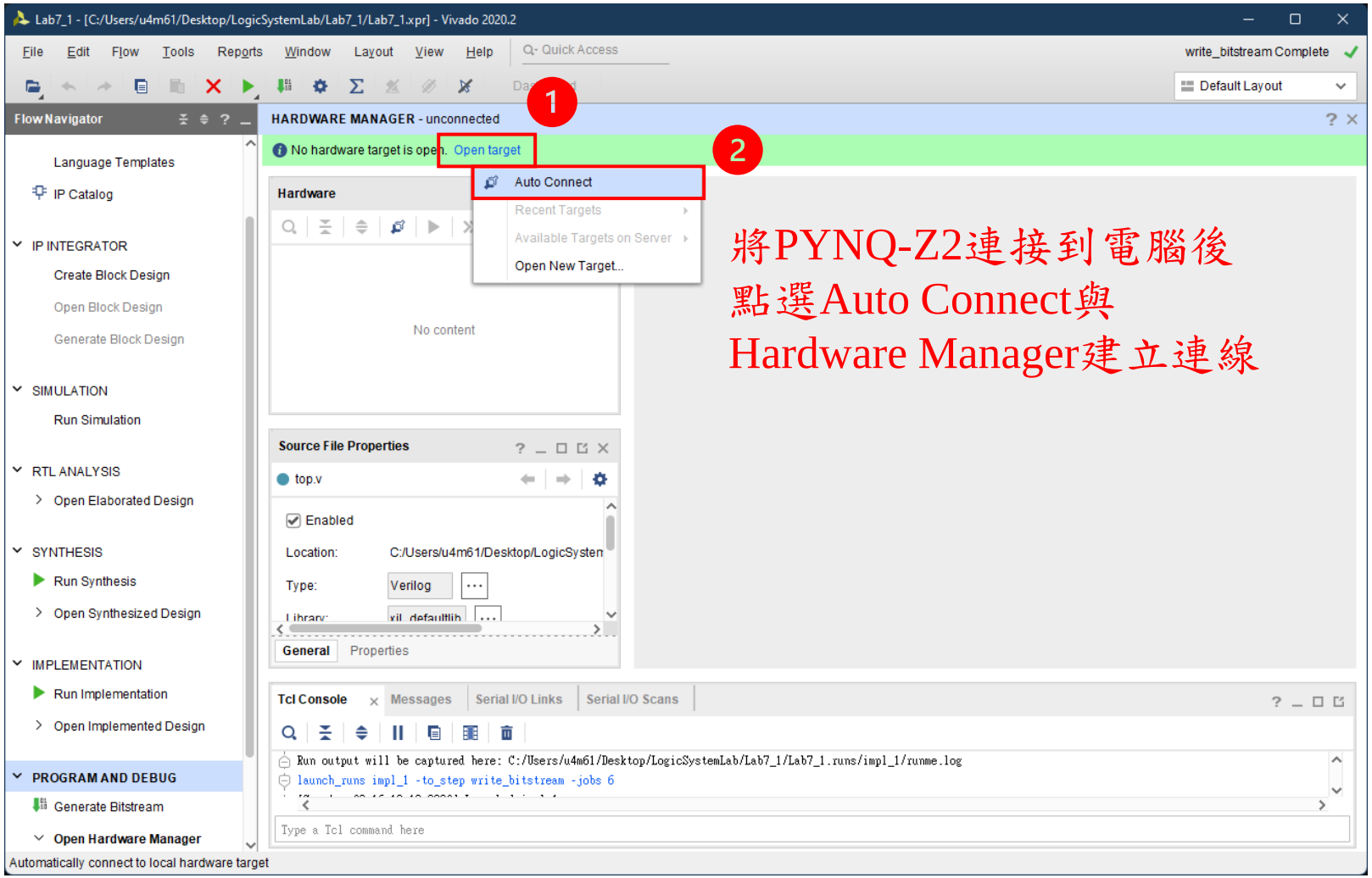


先確認開關在OFF的狀態再連接USB線到電腦

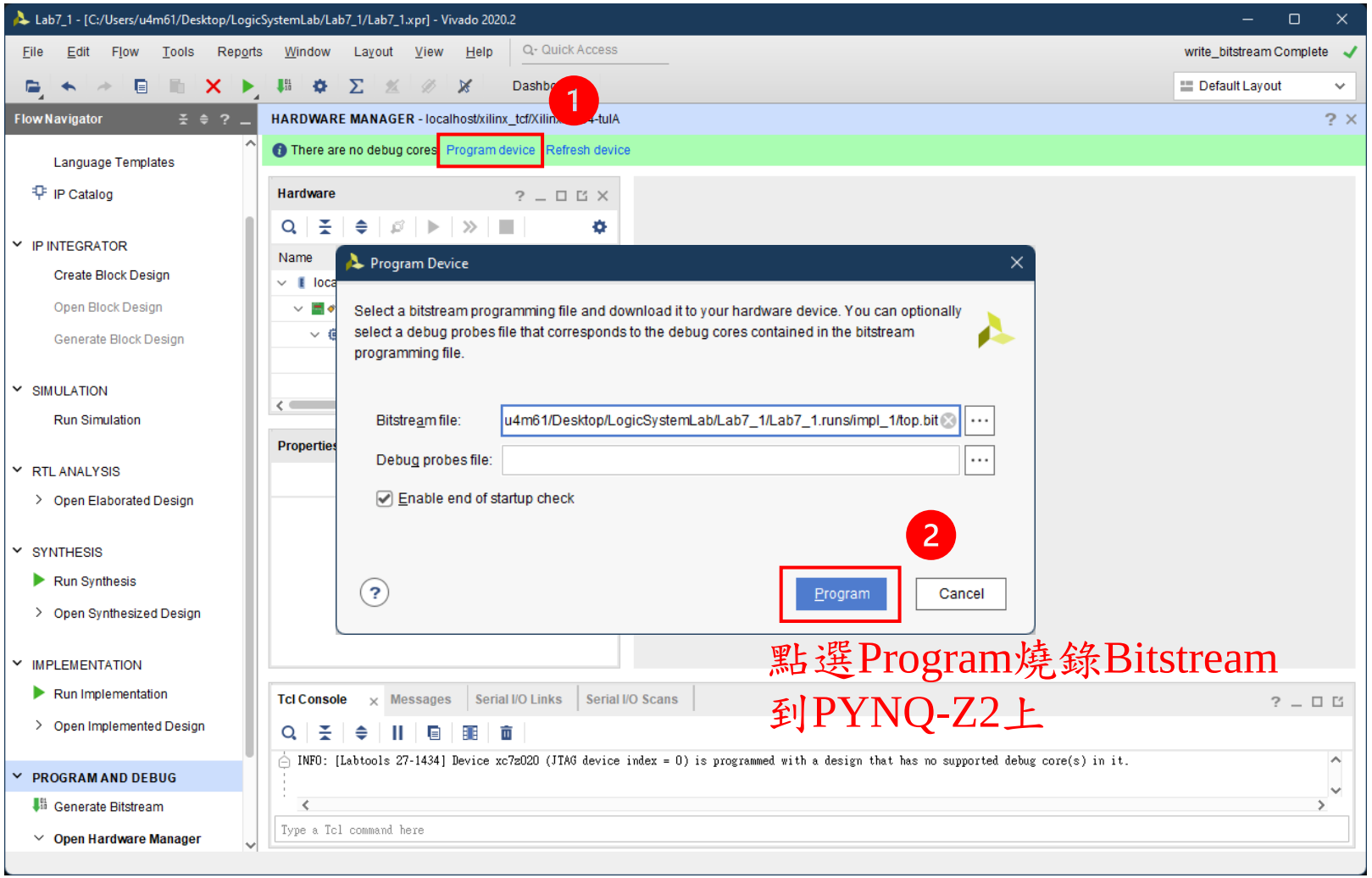
連接PYNQ-Z2



燒錄Bitstream到PYNQ-Z2上

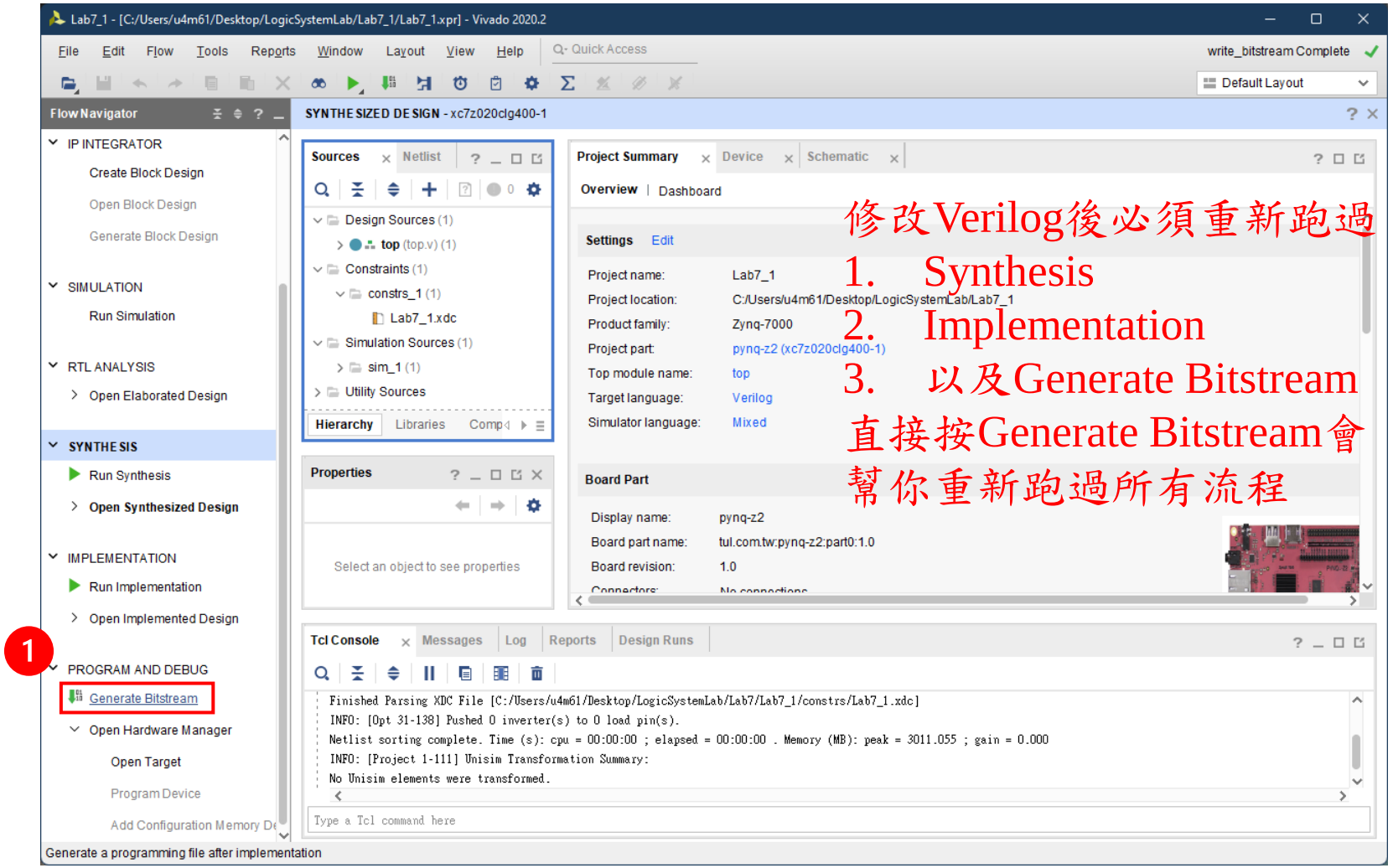


燒錄Bitstream到PYNQ-Z2上



點選Program燒錄Bitstream到PYNQ-Z2上

提示一

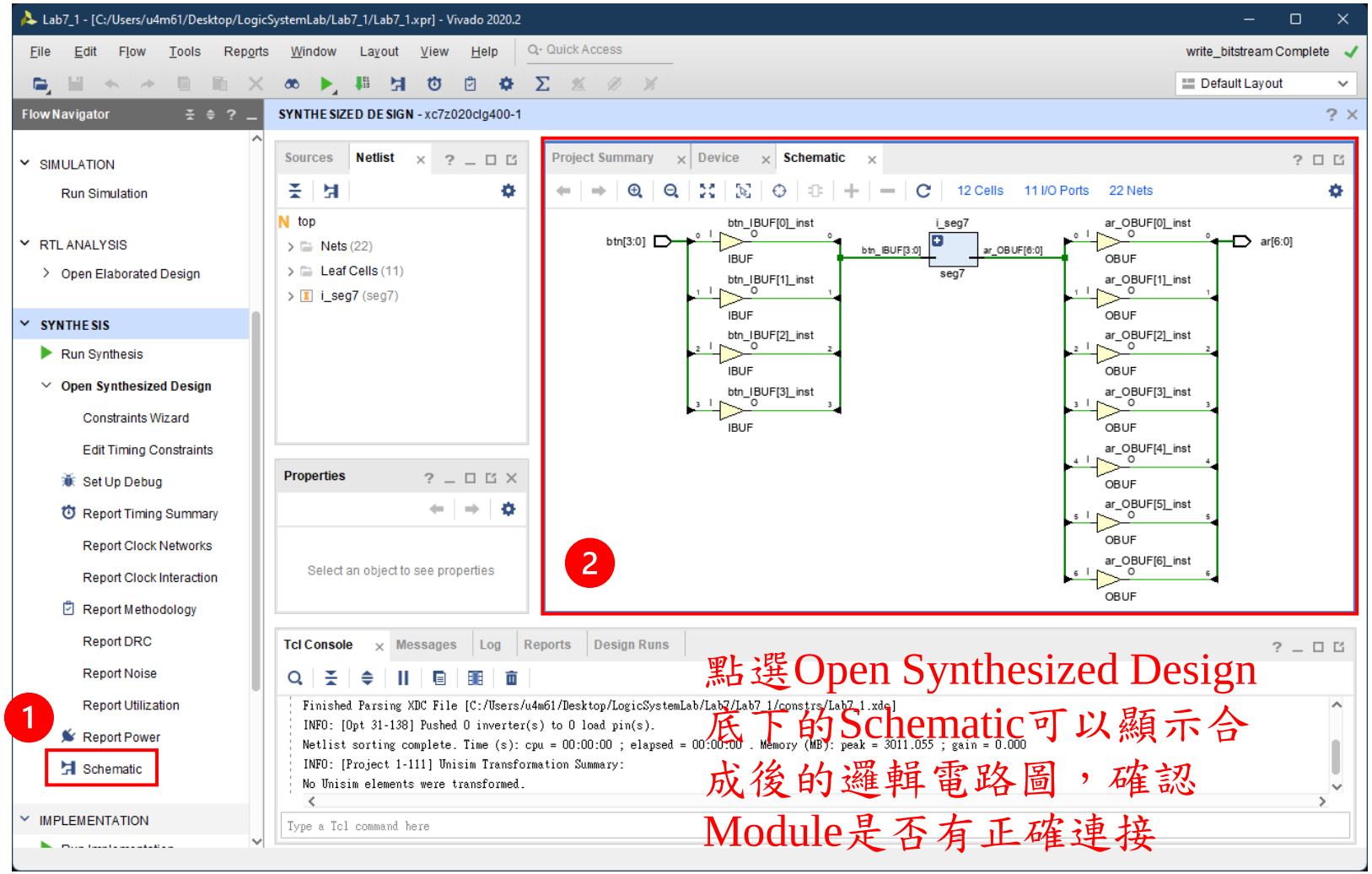


修改Verilog後必須重新跑過

1. Synthesis
2. Implementation
3. 以及Generate Bitstream

直接按Generate Bitstream會幫你重新跑過所有流程

提示二



點選Open Synthesized Design
底下的Schematic可以顯示合
成後的邏輯電路圖，確認
Module是否有正確連接