Example Report

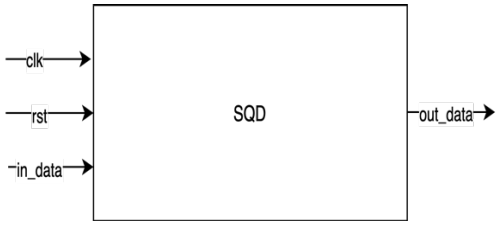
*(格式不用一模一樣，只是列出 **report** 要求的五個點大概所需之內容)*

a. Introduce how you define the circuit

- 此 sequence detector 為 overlap one pattern 的 sequence detector。
- 可以偵測連續不同 cycle 的輸入，當連續三個 cycle 拿到的值為 101 時，下一個 cycle 就會輸出 1

  ……

  ……
- 電路 input/output port :




```
module SQD (
    clk,
    rst,
    in_data,
    out_data,
);

    input clk,rst,in_data;
    output out_data;
```

in_data : …

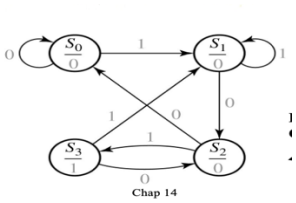
clk : ….

rst : ….

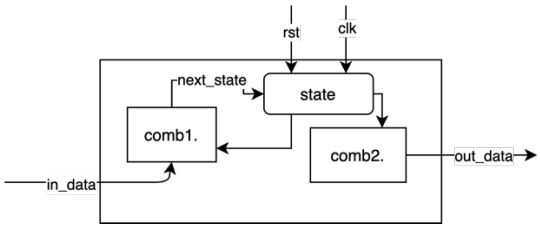
out_data : ….

b. State machine and hardware block diagram

- State machine



- Block diagram



- Asyncronize reset 的電路，程式碼怎麼實現…….
- …..

c. Verify

寫了 c++ 程式碼產生 input 輸入給 testbench 跟對應的 golden 驗證結果是不是正確，解釋程式碼…

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d. Result

```
----------------------------------------------------
START!!! Simulation Start .....
----------------------------------------------------
input= 1, out data equal to 0
input= 0, out data equal to 0
input= 1, out data equal to 0
input= 1, out data equal to 1
input= 1, out data equal to 0
input= 0, out data equal to 0
input= 1, out data equal to 0
input= 1, out data equal to 1
input= 0, out data equal to 0
input= 1, out data equal to 0
----------------------------------------------------
Simulation END, SUCCESS!!!
----------------------------------------------------
```

這是在 terminal 輸成功的結果，output 正確

```
----------------------------------------------------
START!!! Simulation Start .....
----------------------------------------------------
input= 1, out data equal to 0
input= 0, out data is 1 but golden is 0
input= 1, out data equal to 0
input= 1, out data equal to 1
input= 1, out data is 1 but golden is 0
input= 0, out data is 1 but golden is 0
input= 1, out data equal to 0
input= 1, out data equal to 1
input= 0, out data is 1 but golden is 0
input= 1, out data equal to 0
----------------------------------------------------
Simulation END, there are some errors.....
----------------------------------------------------
```

驗證失敗的結果 會顯示應該正確的值…

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e. What you learn

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