Logic Design System Lab Final Project - Sequence Detector

Deadline : 2021/06/22 11:59:59 pm

1. Description

In digital IC design, these steps are usually done at RTL simulation level before getting further to synthesis and layout:

a. Define: Define the specification of this product. In this step, the functionality and the purpose of the design is specified. Furthermore, some limitations must be defined to restrict the product to achieve a certain level.
b. Design: Based on the SPEC, RTL designers design and implement the micro-architecture of the circuits and must meet the requirement.
c. Verify: Design Verification Engineers (DV engineers) will design a verification environment to verify the design. Some methodology can be used such as direct and random testing.

In this project, each of teams will act like an RTL team and designs a sequence detector. This circuit takes a sequence of 1 and 0 as input, and it asserts the output once detecting a certain input pattern. It can either detector overlapped or non-overlapped patterns. Examples are shown at the end of this section.

Please follow the concept from the examples and design a sequence detector which can either detect one sequence longer than 3 bits(>=4) or detect getter than 1 patterns (>=2). You should follow the concepts of those three steps described above. First, define your design. I/O communication and functionality should be considered in this step. Secondly, design the state machine (moore or mealy) and consider the micro-architecture (modules, components, wire connections) that will be used in this circuit. Finally, design the testbench that can verify your design. The testbench should feed some testing data into your circuit and check the correctness of the result. (More information of the squence detector can be found in "*Lecture 13 Derivation of State Graphs and Tables*")

**Examples A(overlap & sequence amount):*

< 1 > Overlapped 101-sequence detector:

input sequence:	1	**1**	**0**	**1**	**0**	**1**	1	**1**	**0**	**1**	**0**	**1**
output sequence:	0	0	0	1	0	1	0	0	0	1	0	1

< 2 > Non-overlapped 101-sequence detector:

input sequence: **1 0 1** 0 1 1 **1 0 1** 0 1

output sequence: 0 0 1 0 0 0 0 0 1 0 0

< 3 > Overlapped 101-110 Double Sequence detector:

input sequence: **1 1 0 1 1 1 0** 0 **1 0 1**

output sequence: 0 0 1 1 0 0 1 0 0 0 1

**Examples B(moore & mealy):*

< 1 > Non-overlapped 101-sequence detector (mealy):

input sequence: **1 0 1** 0 1 1 **1 0 1** 0 1

output sequence: 0 0 1 0 0 0 0 0 1 0 0

< 2 > Non-overlapped 101-sequence detector (moore):

input sequence: **1 0 1** 0 1 1 **1 0 1** 0 1

output sequence: 0 0 0 1 0 0 0 0 0 1 0

2. Report Requirement

a. Introduce how you define the circuit. Please describe the I/O ports and functionality (eg. show the input and output pattern).

b. Introduce how you design the circuit. Please draw the state diagram and explain how your hardware works. You can draw block diagrams to explain your hardware.

c. Introduce how you verify the design. Please show the design of your testbench and testing data (and how you generate it).

d. Show screenshots of your result (or share the problems you had).

e. Share what you learned from this course.

3. Scoring

a. RTL Hardware Design (30%)

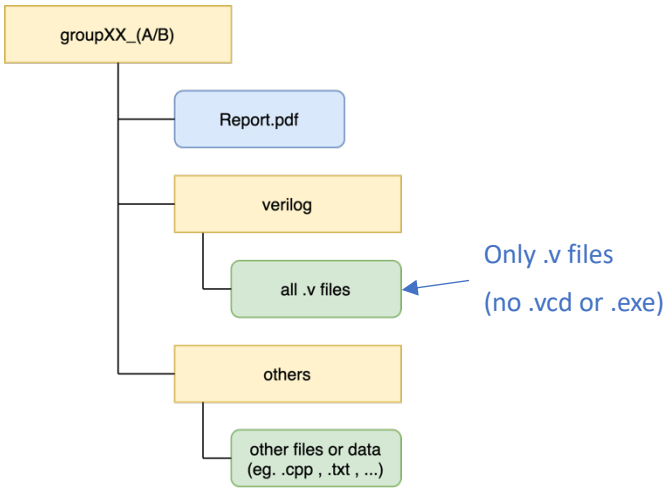
b. Testbench verification (20%)

c. Report (30%)

d. Demo (20%)

4. Submission & DEMO

a. Please hand in the file with the folder tree template beneath, and compress it into "*groupXX_(A/B).zip*"



b. Hand in the file by email: ericwang0911@gmail.com , and arrange a time for demo before deadline (as soon as you finish the project).