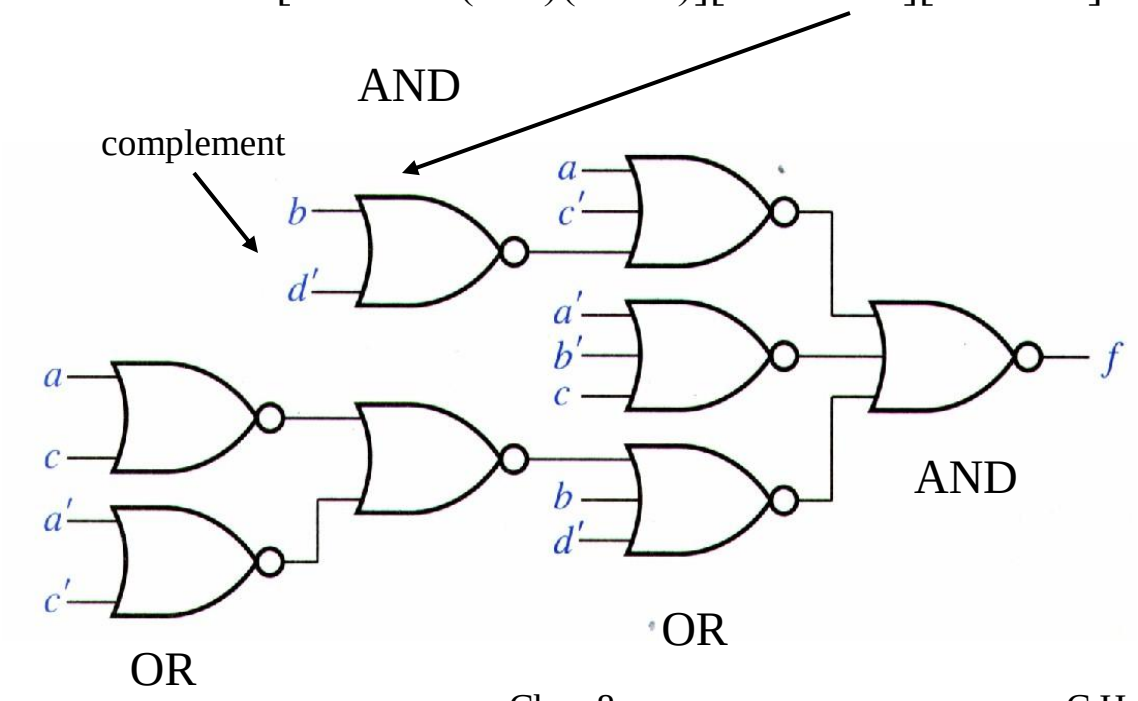
Lecture 8 Combinational Network Design and Issues

- Limited gate fan-in
  - Using 3-input NOR gates.
- Example : f (a,b,c,d) = Σm(0,3,4,5,8,9,10,14,15)
  - f’= a’b’c’d + ab’cd + abc’ + a’bc + a’cd’ (2 4-input, 1 5-input)
  - f’ = b’d(a’c’+ac) + a’c(b+d’) + abc’ (use common terms)
  - f = [b + d’ + (a+c)(a’+c’)][a+c’+b’d][a’+b’+c]



Multiple-Output With Limited Fan-In

- Using only 2-input NAND.

$f_1 = b'c' + ab' + a'b$

$f_2 = b'c' + bc + a'b$

$f_3 = a'b'c + ab + bc'$

- 3-input OR-gate

$f_1 = b'(a+c') + a'b$

$f_2 = b(a'+c) + b'c'$ or $(b'+c)(b+c') + a'b$ ↙ Choose this because of common term

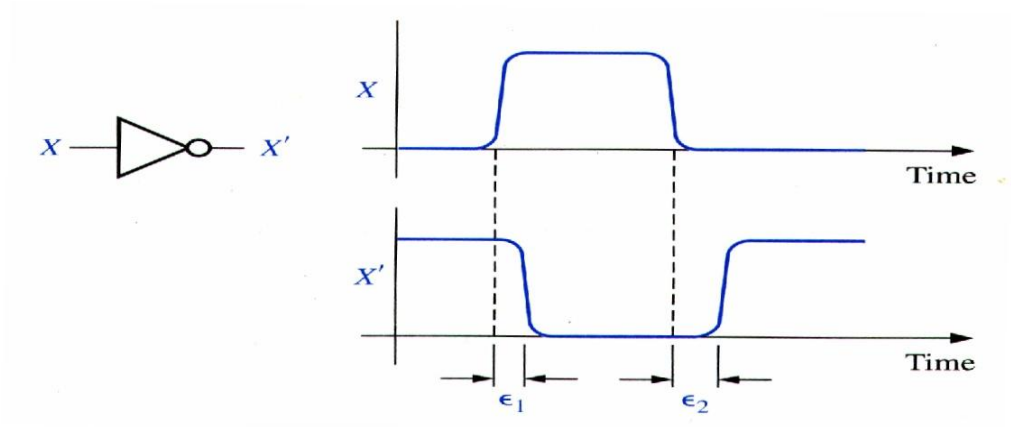
$f_3 = a'b'c + b(a+c') = a'(b+c')' + b(a+c')$

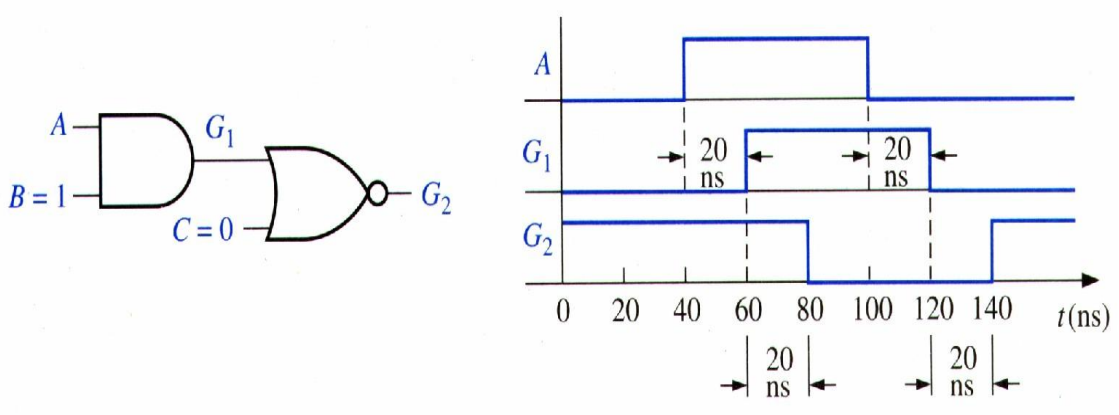
↖ 3 inputs

↗ 2 inputs

Gate Delay

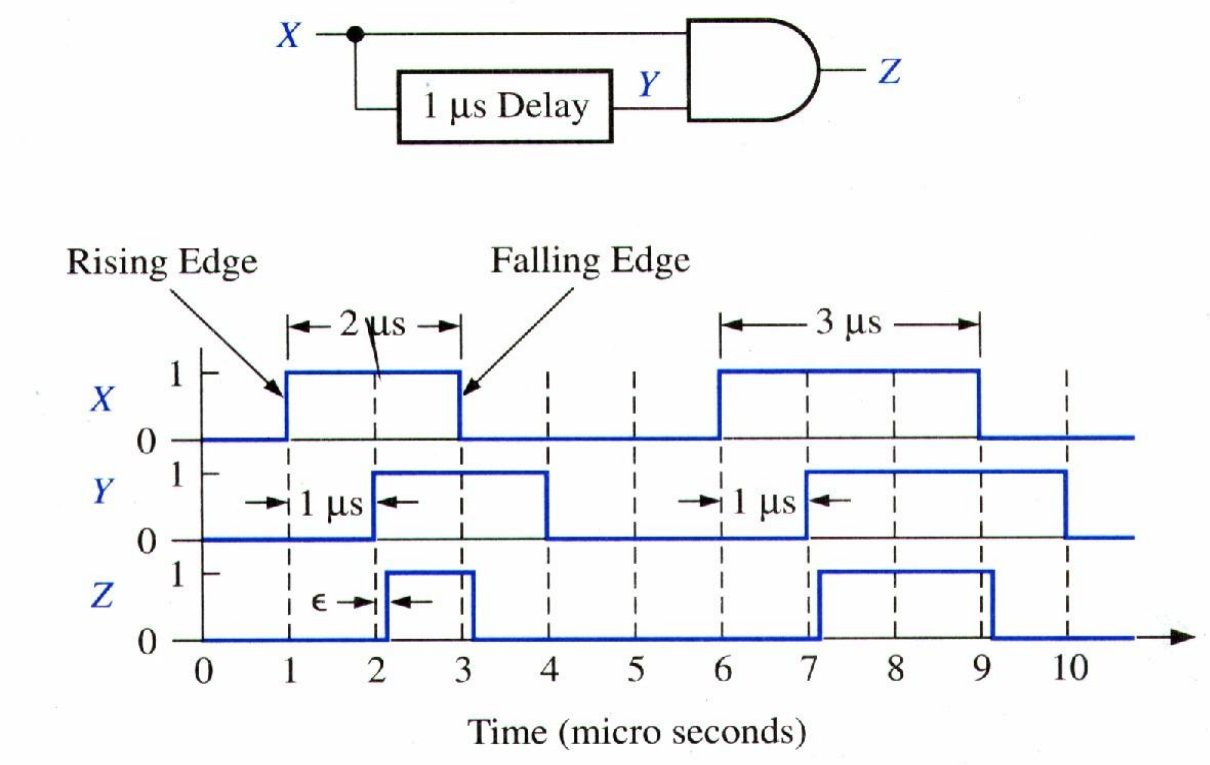
- Propagation delay
- Timing diagram





Network Delay

- Delay element
  - Extra logic circuit, capacitance.



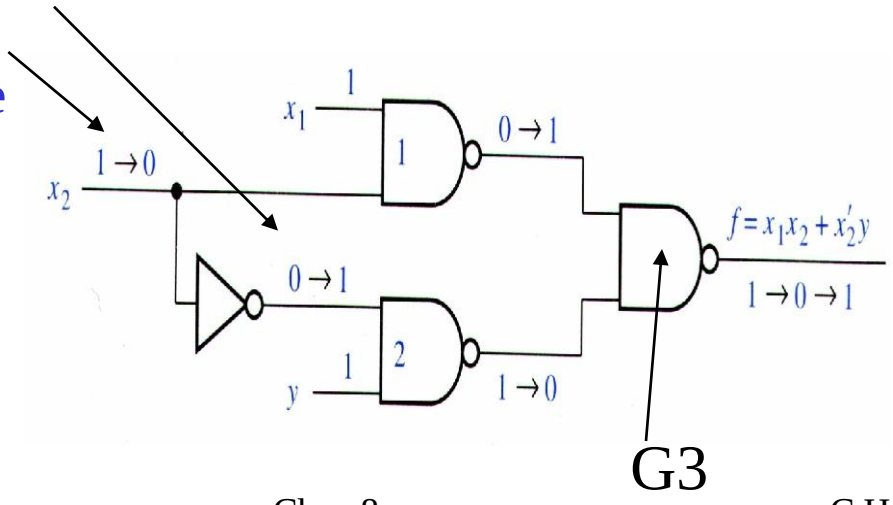
Hazards

- Uncertain delays in logic circuits have the ability to introduce temporary or transient signal pulse where none are supposed to exist.
  - The spurious pulses or noise signals are referred to as **glitches**.
  - A **glitch** is a momentary error condition on the output of a circuit due to unequal signal delay paths in the circuit.
  - A glitch is identified as an additional pulse or pulses on output.
  - The circuit conditions that allow such signals to appear are called **hazards**.
  - A circuit with a hazard may or may not produce glitches, depending on the input patterns and the electrical charactersitics of the circuit.

An Example of Hazard

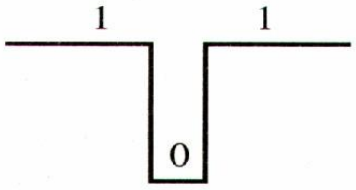
- Propagation delays result in output transients.
  - When x_2 1->0, the output should remain to 1.
    - But if G1 goes to 1 first, then (11) for G 3 results in 0 output. Suppose that G2 has a longer delay, then (1,0) causes the output back to 1.

x_2 and x_2' have the same value for a short time.

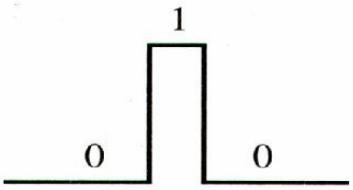


Static and Dynamic Hazard

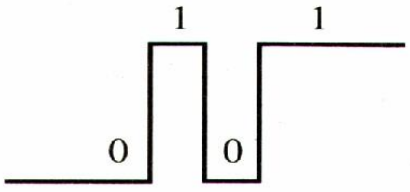
- Hazard
  - In a combinational part of a sequential network, hazard can cause the sequential network to malfunction.
  - Hazard in an output network can cause a problem if the output serves as the input to another asynchronous network.

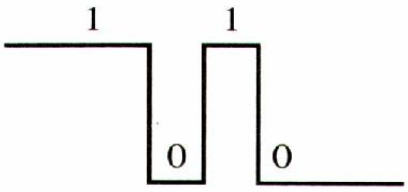


(a) Static 1-hazard



(b) Static 0-hazard





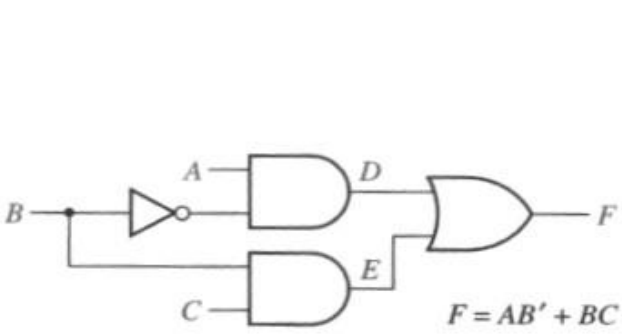
(c) Dynamic hazards

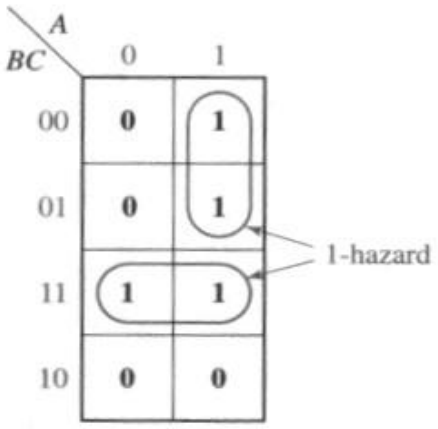
Glitch Eliminations

- If the glitches are narrow in width, they might be filtered out by the inertial property of physical gates.
- Hazard controls are only feasible to fairly small circuits that operate under restrictive conditions.
  - Avoid multiple simultaneous input changes. (Restriction)

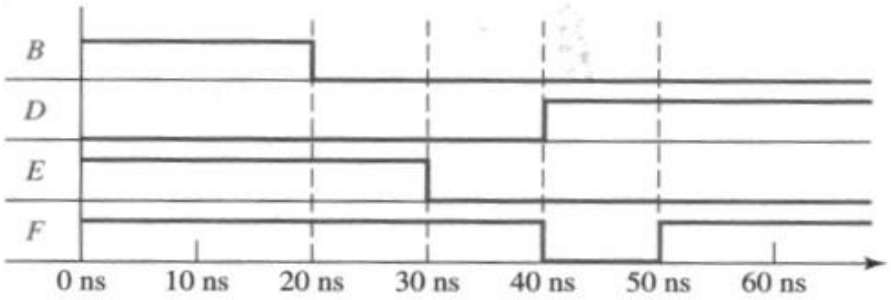
Hazard Detection

- 1-hazard





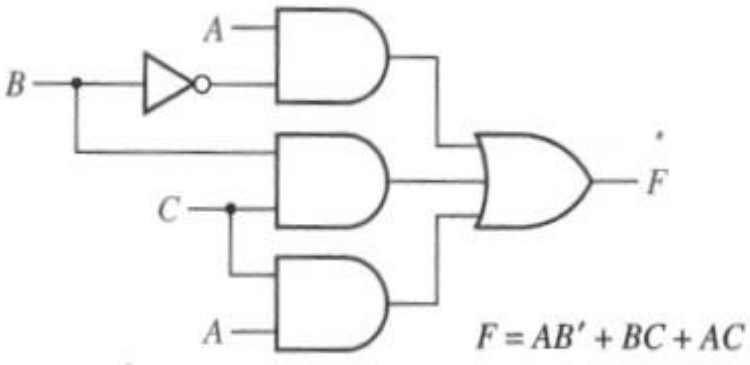
(a) Circuit with a static 1-hazard

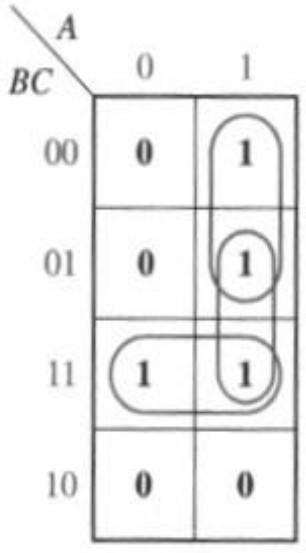


(b) Timing chart

Remove the Hazard

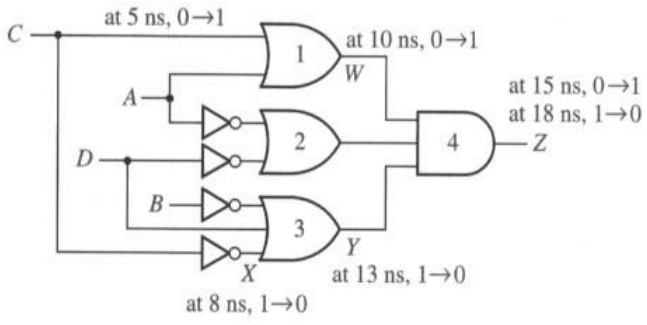
– Add a redundant gate to remove the hazard.



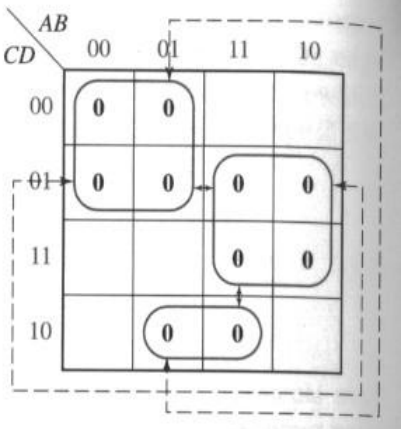


Hazard Detection (cont.)

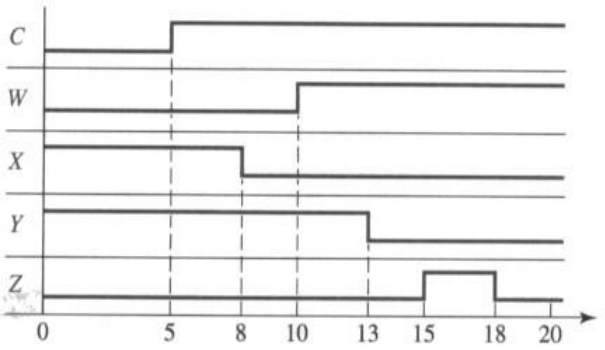
- Static 0-hazard



(a) Circuit with a static 0-hazard



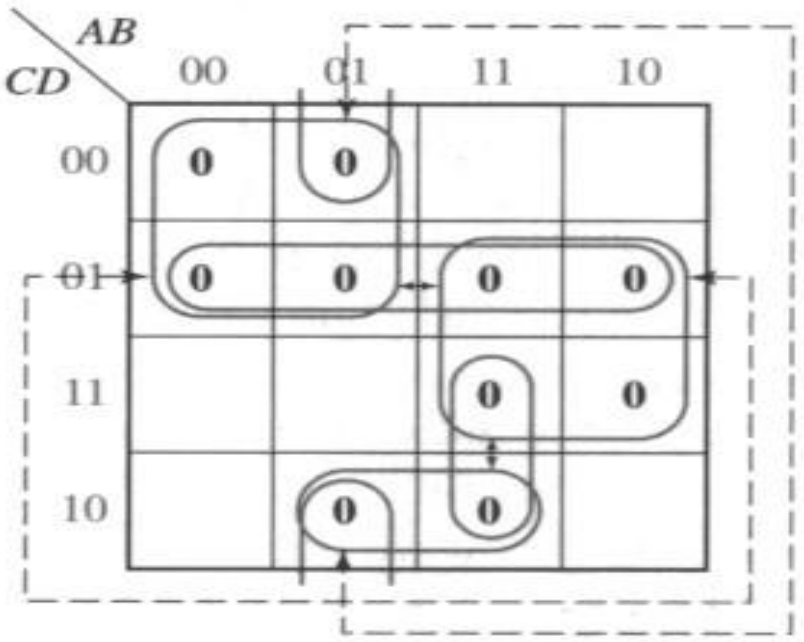
(b) Karnaugh map for circuit of (a)



(c) Timing diagram illustrating 0-hazard of (a)

Remove Hazard

- Looping additional prime implicants that cover the adjacent 0's that are not already covered by a common loop.



Possible Causes for Errors

- Incorrect design
- Gate connected wrong
- Wrong inputs to the network
- Defective gates
- Defective wires

  stuck at zero
  stuck at one