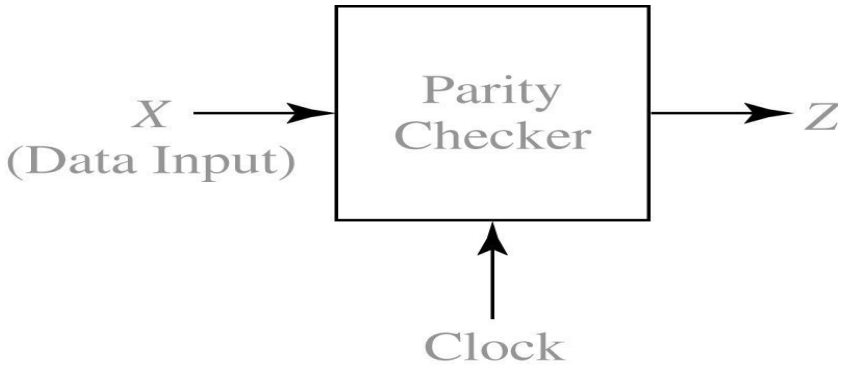
Lecture 12
Analysis of Clocked Sequential Network

- Given a sequential network and input sequence, analyze the network to determine the FF state sequence and output sequence.
  - First by tracing the 1 and 0 signals through the network.
  - Next by constructing a state graph or state table to represent the behavior of the network.

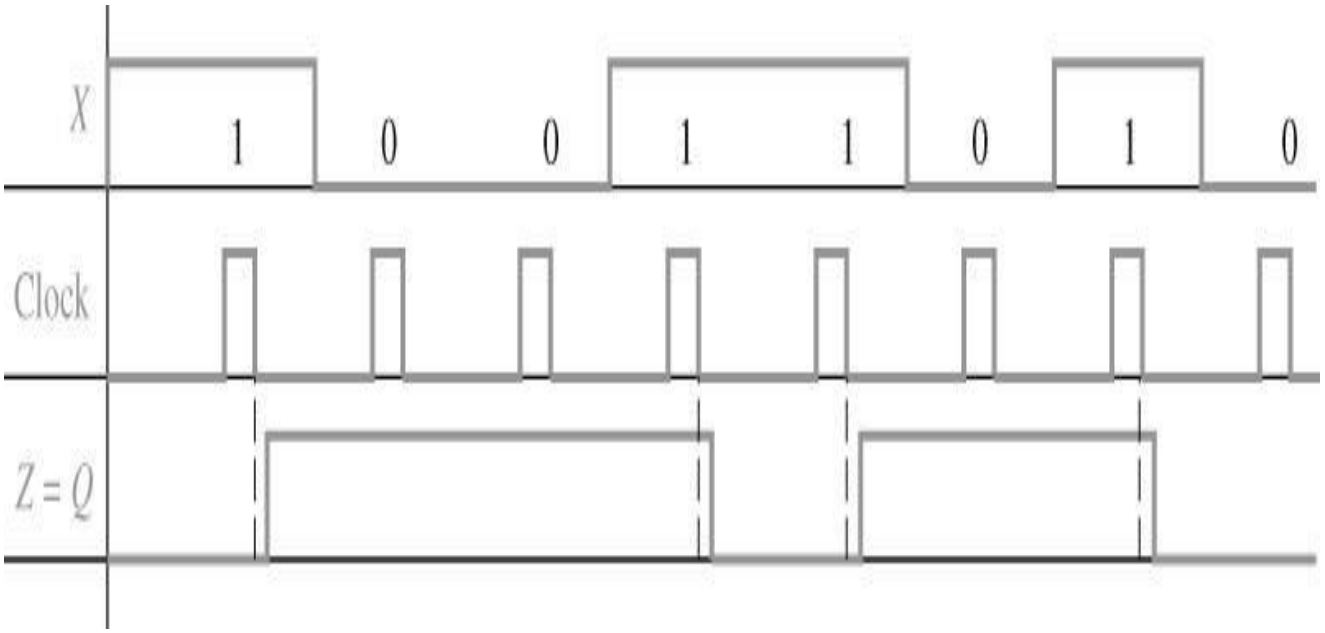
A Sequential Parity Checker

- Parity
  - Odd parity and even parity.
    - Add 1or 0 to a datum so that the total number of 1's is odd (odd parity) or even (even parity).
  - Error detection.
- Example
    - Serial data input, one bit at a time.
    - Output Z = 1 if total number of 1 inputs received is odd.
    - If the input is odd parity, and the final output Z = 1. This is correct.
    - A final output Z = 0 indicates that an error in transmission has occurred.



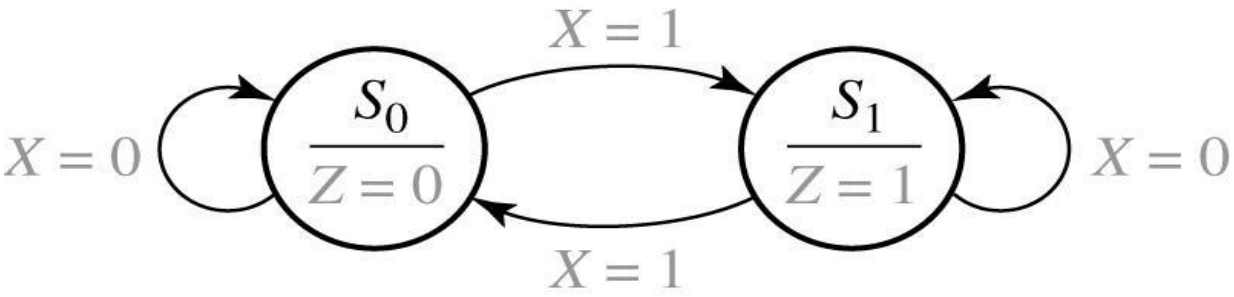
A Sequential Parity Checker (cont.)

- Assume that X is synchronized with the clock and changes only between clock pluses.
- X is determined at the active clock edge.
- Clock input is used to distinguish consecutive 0's or 1's.



A Sequential Parity Checker (cont.)

- A state graph
  - S0: even number of 1's received
  - S1: odd number of 1's received.



- State table

Table 13–1

State Table for Parity Checker

(a)

Present State	Next State $X=0$	Next State $X=1$	Present Output
S_0	S_0	S_1	0
S_1	S_1	S_0	1

(b)

Q	Q^+ $X=0$	Q^+ $X=1$	T $X=0$	T $X=1$	Z
0	0	1	0	1	0
1	1	0	0	1	1

A Sequential Parity Checker (cont.)

- Two states are required. We can use a FF.
  - A T FF can be used. When Q and Q^+ differs, T = 1. Note that T is input to FF. Both Q and Q^+ are outputs of the FF. (Homework: Use a D FF)
  - In the table, when X = 1 , T = 1, so T = X.

Table 13–1

State Table for Parity Checker

(a)

Present State	Next State $X=0$	Next State $X=1$	Present Output
S_0	S_0	S_1	0
S_1	S_1	S_0	1

(b)

Q	Q^+ $X=0$	Q^+ $X=1$	T $X=0$	T $X=1$	Z
0	0	1	0	1	0
1	1	0	0	1	1

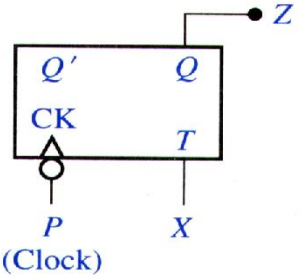


Figure 13–4

Analysis by Signal Tracing and Timing Charts

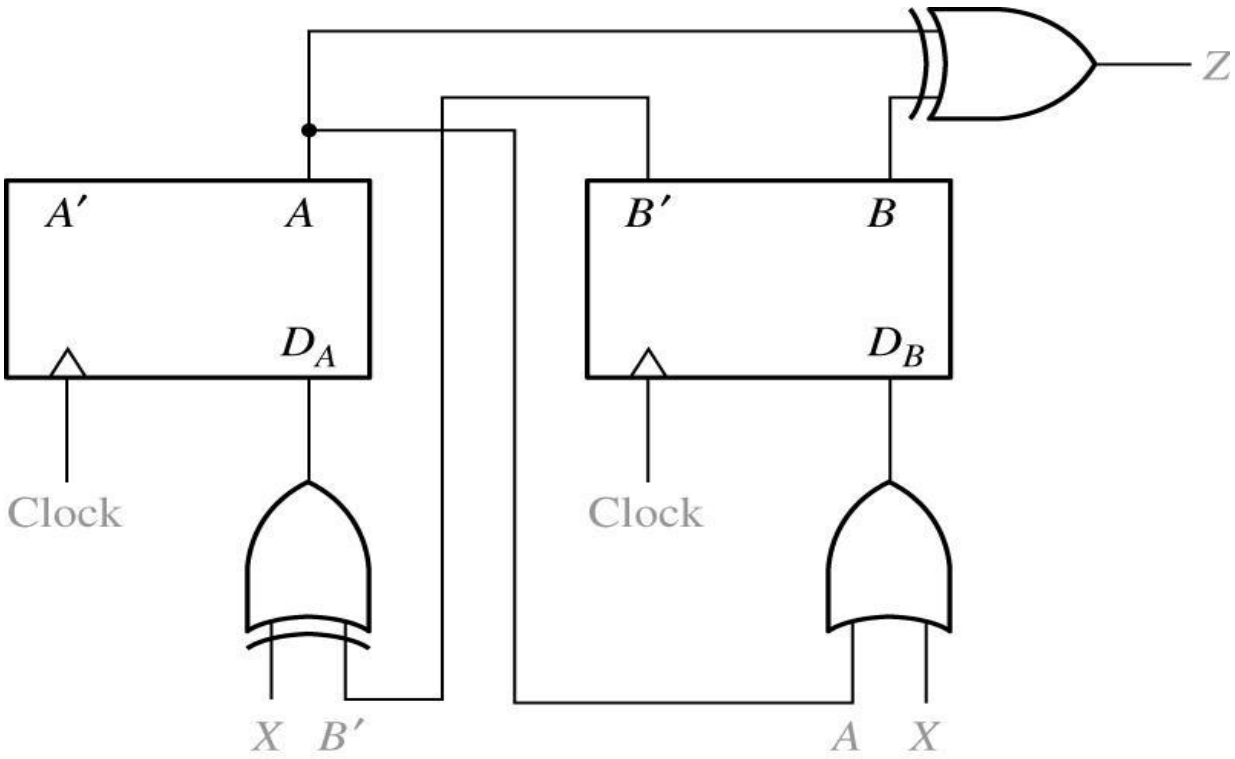
- Given a clocked sequential network, procedure for analysis is as follows:
  - Assume initial state (0) for FF.
  - For the first input in the given sequence, determine the network output and the FF inputs.
  - Apply clock to the FFs and determine the new FF states after the next active clock edge.
  - Determine the outputs due to the new state.
  - Repeat for each input in the given sequence sequence.

  – This is a timing chart.

Moore Machine

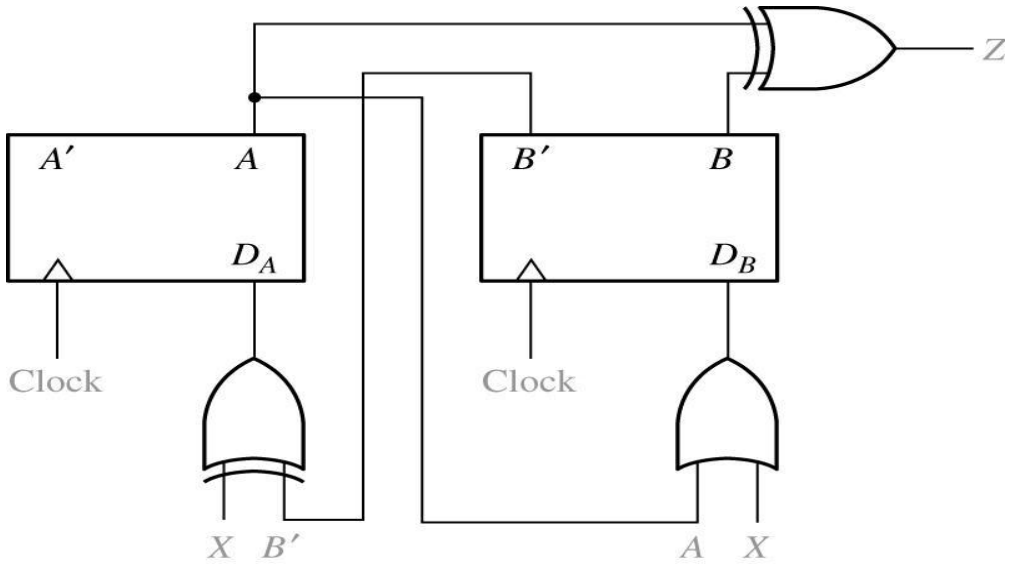
– Output depends on only the present state of FF. This network is referred to as a Moore machine. (Output displaces w.r.t. input in Moore network)

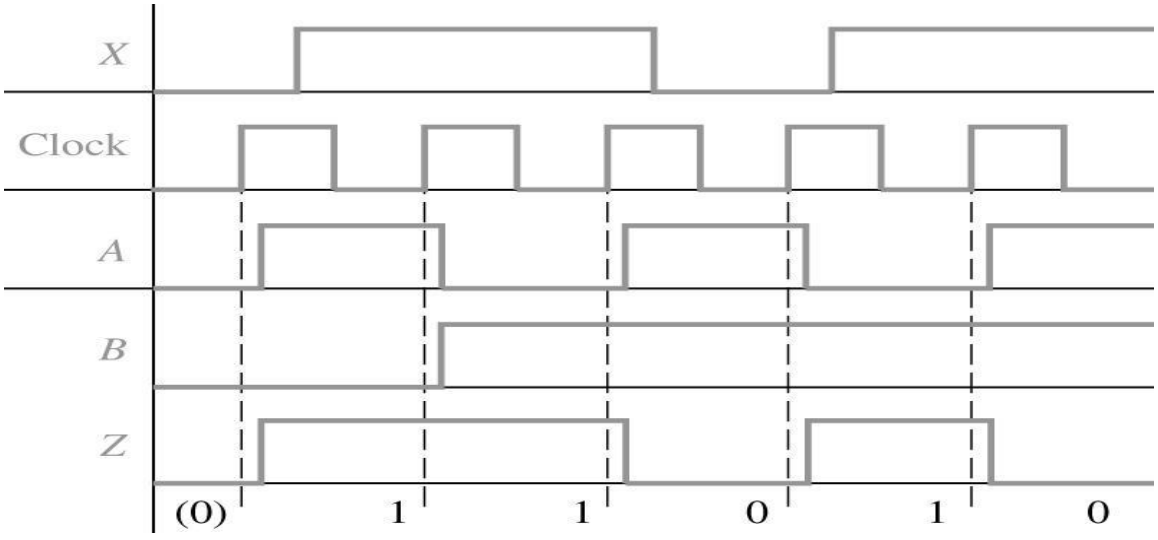
- X = 0 1 1 0 1
- A = 0 1 0 1 0 1
- B = 0 0 1 1 1 1
- Z= (0)1 1 0 1 0



Moore Machine (cont.)

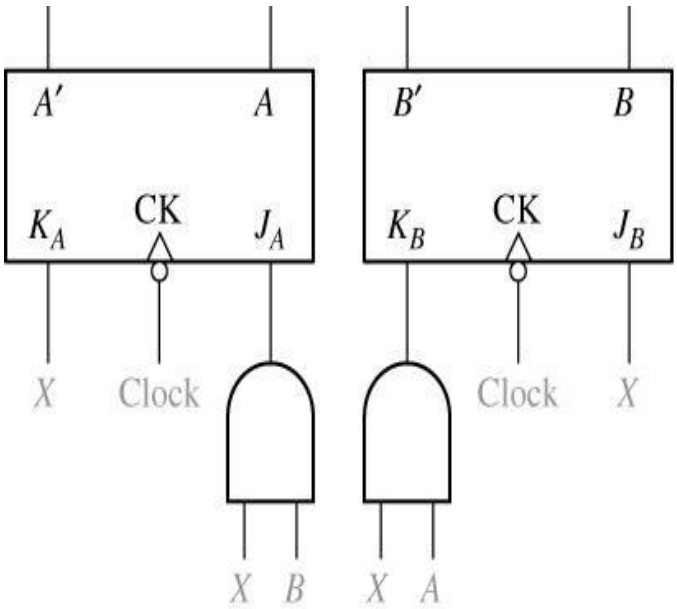
- Assume X = 01101
  - Initially, X = 0, D_A = 1, D_B = 0. So after rising clock edge, A = 1, and B = 0.

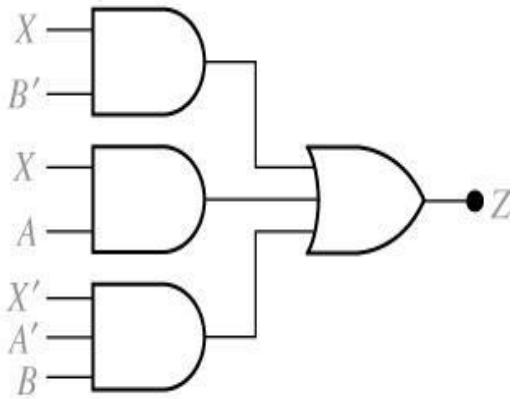




Mealy Machine

- Output depends on the input and the FF states. That is, Z may change either when input changes or the FF state changes.
- Example: Output does not displace w.r.t input. Input dominates.





Mealy Machine (cont.)

- X = 1 0 1 0 1
- A = 0 0 0 1 1 0
- B = 0 1 1 1 1 0
- Z = 1(0)1 0(1)0 1 (glitches or spikes)

False 0 output

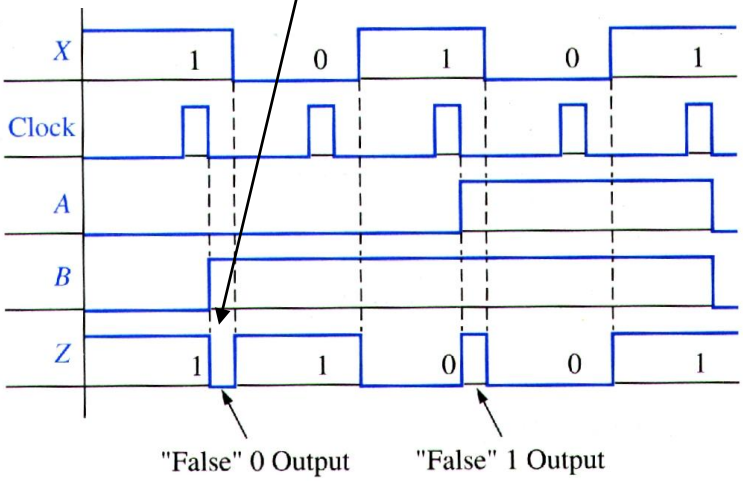
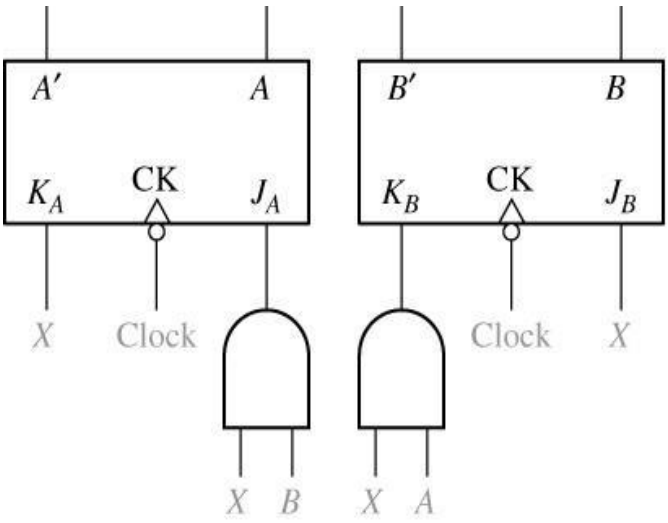
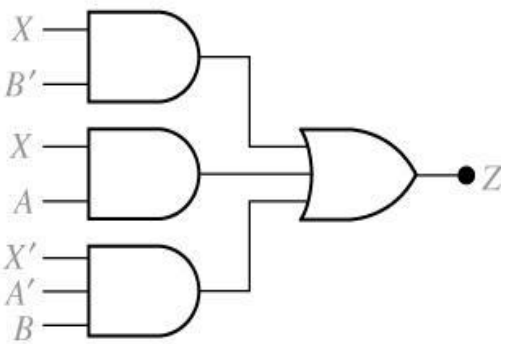


Figure 13–8
Timing Chart for Network of Fig. 13–7





State table and graph constructions

- State table constructions
  - Network inputs, present state, and next state.
    - Determine the FF input equation and output equations.
    - Derive the next-state equations for each FF from its input equations using
      - $Q^+ = D$
      - $Q^+ = T \oplus Q$
      - $Q^+ = S+R'Q$
      - $Q^+ = JQ' + K'Q$
    - Plot a next-state map
    - Combine these maps to form state table. (This is also called a transition table.)

Example: State Table

- Step (Moore machine)
  - Input equations and output equation
    - $D_A = X \oplus B'$, $D_B = X + A$, $Z = A \oplus B$
  - Next state equations
    - $A^+ = X \oplus B'$
    - $B^+ = X + A$
  - Next state K map: $A^+ = f(A, B, X)$. A next state = function of present states and inputs

AB \ X	0	1
00	1	0
01	0	1
11	0	1
10	1	0

A^+

AB \ X	0	1
00	0	1
01	0	1
11	1	1
10	1	1

B^+

Example: State Table (cont.)

- Moore State table

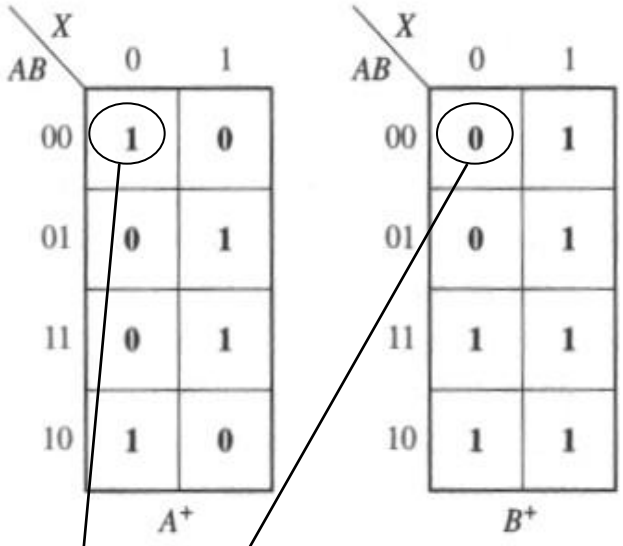


TABLE 13-2 Moore State Tables for Figure 13-5

(a)

AB	A^+B^+ X = 0	X = 1	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

(b)

Present State	Next State X = 0	X = 1	Present Output (Z)
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1

State Graph

- Moore State graph

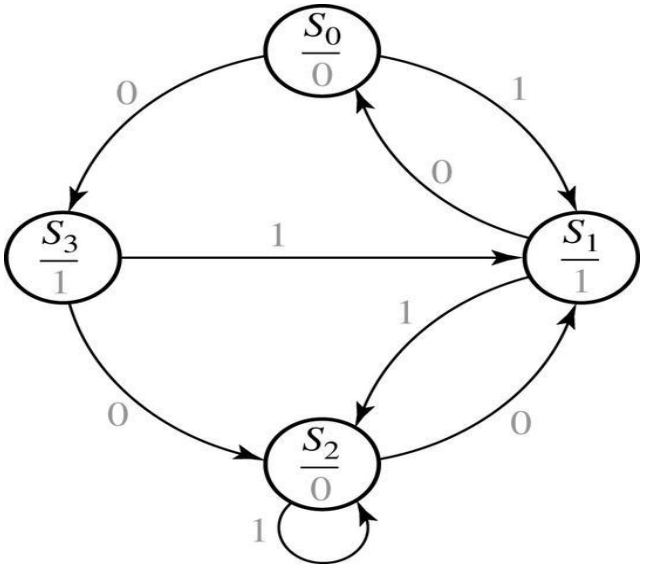


TABLE 13-2 Moore State Tables for Figure 13-5

(a)

AB	A^+B^+ X = 0	A^+B^+ X = 1	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

(b)

Present State	Next State X = 0	Next State X = 1	Present Output (Z)
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1

Mealy Machine Example

- Next state equation
  - $A^+ = J_A A' + K_A'A = XBA' + X'A$
  - $B^+ = J_B B' + K_B'B = XB' + (AX)'B = XB' + X'B + A'B$
  - $Z = X'A'B + XB' + XA$

AB \ X	0	1
00	**0**	**0**
01	**0**	**1**
11	**1**	**0**
10	**1**	**0**

A^+

AB \ X	0	1
00	**0**	**1**
01	**1**	**1**
11	**1**	**0**
10	**0**	**1**

B^+

AB \ X	0	1
00	**0**	**1**
01	**1**	**0**
11	**0**	**1**
10	**0**	**1**

Z

Mealy Machine Example

- State table

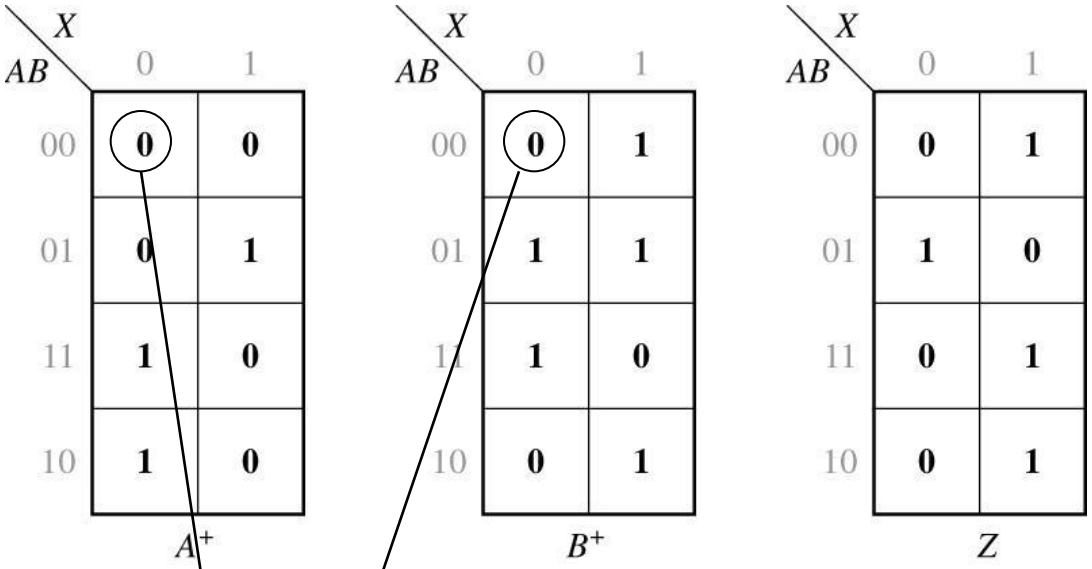


TABLE 13-3 Mealy State Tables for Figure 13-7

(a)

AB	A^+B^+ X = 0	A^+B^+ X = 1	Z X = 0	Z X = 1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

(b)

Present State	Next State X = 0	Next State X = 1	Present Output X = 0	Present Output X = 1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

Example: Mealy Machine (cont.)

- Mealy state graph
  - If present input changes, the output will changes *immediately*. But the present state will not change until after the clock edge.

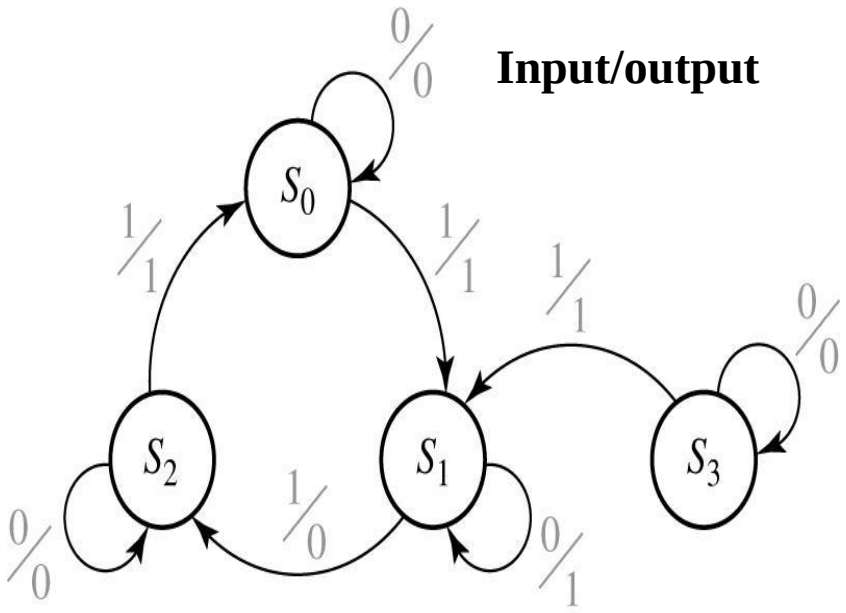


TABLE 13-3 Mealy State Tables for Figure 13-7

(a)

AB	A^+B^+ X = 0	1	Z X = 0	1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

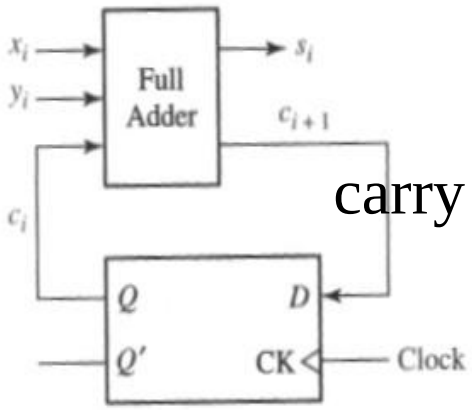
(b)

Present State	Next State X = 0	1	Present Output X = 0	1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

A Serial Adder

- Two operands are fed in serially beginning at x_0, y_0 (store carry)

FIGURE 13-12
Serial Adder

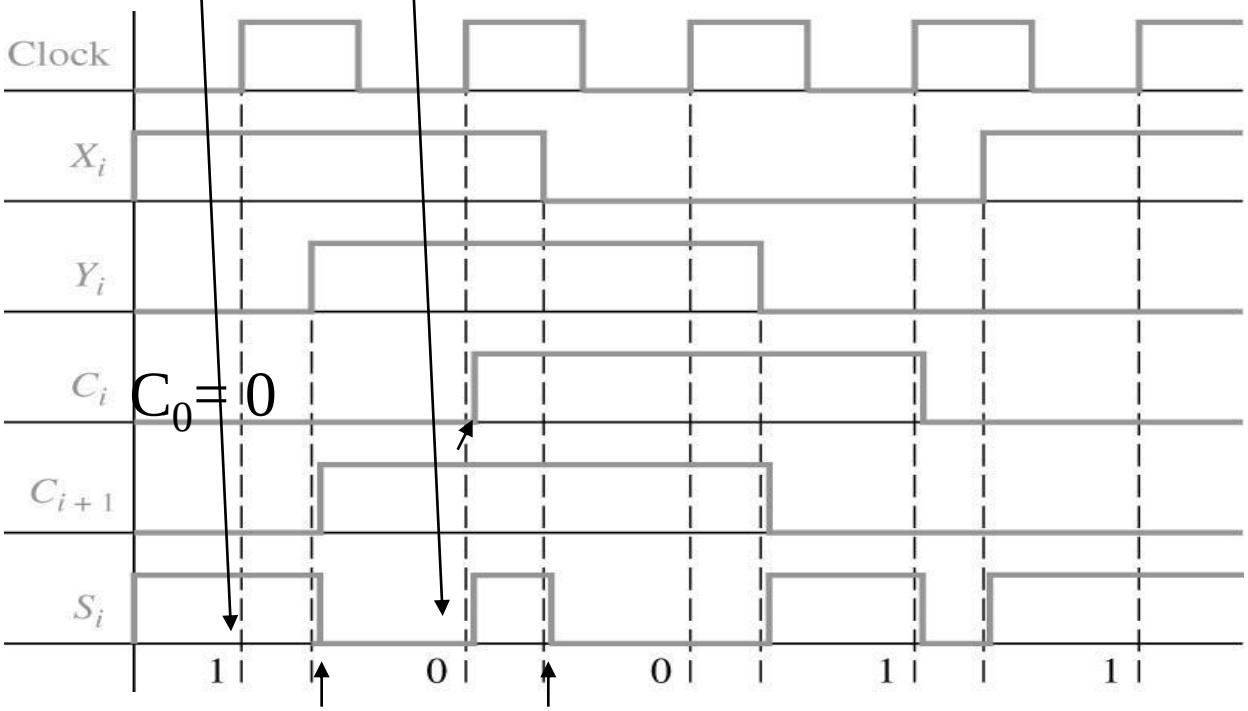


(a) With *D* flip-flop

x_i	y_i	c_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(b) Truth table

Read answer (s) before the rising edge



Serial Adder

- Mealy machine (S_0 c_i = 0, S_1: c_i = 1)

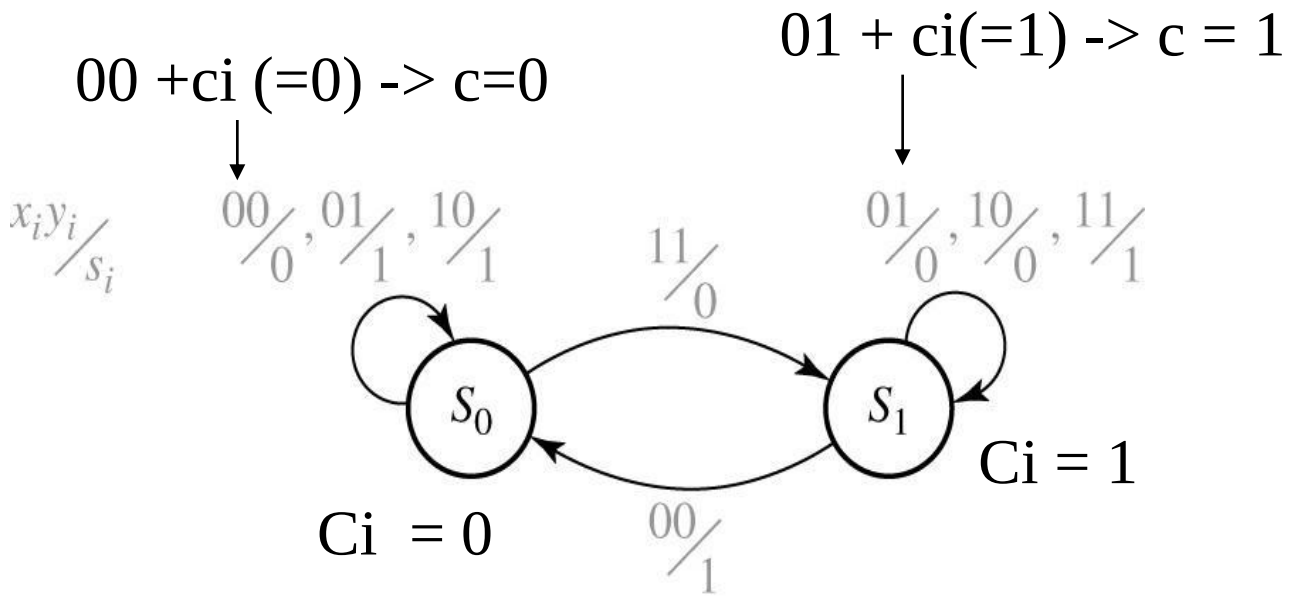
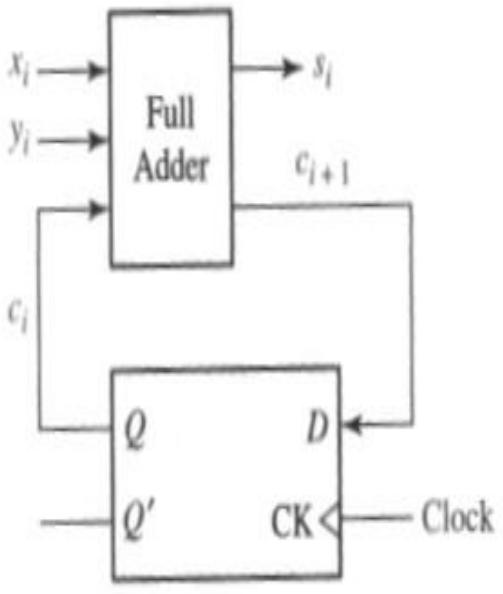


FIGURE 13-12
Serial Adder



(a) With *D* flip-flop

x_i	y_i	c_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

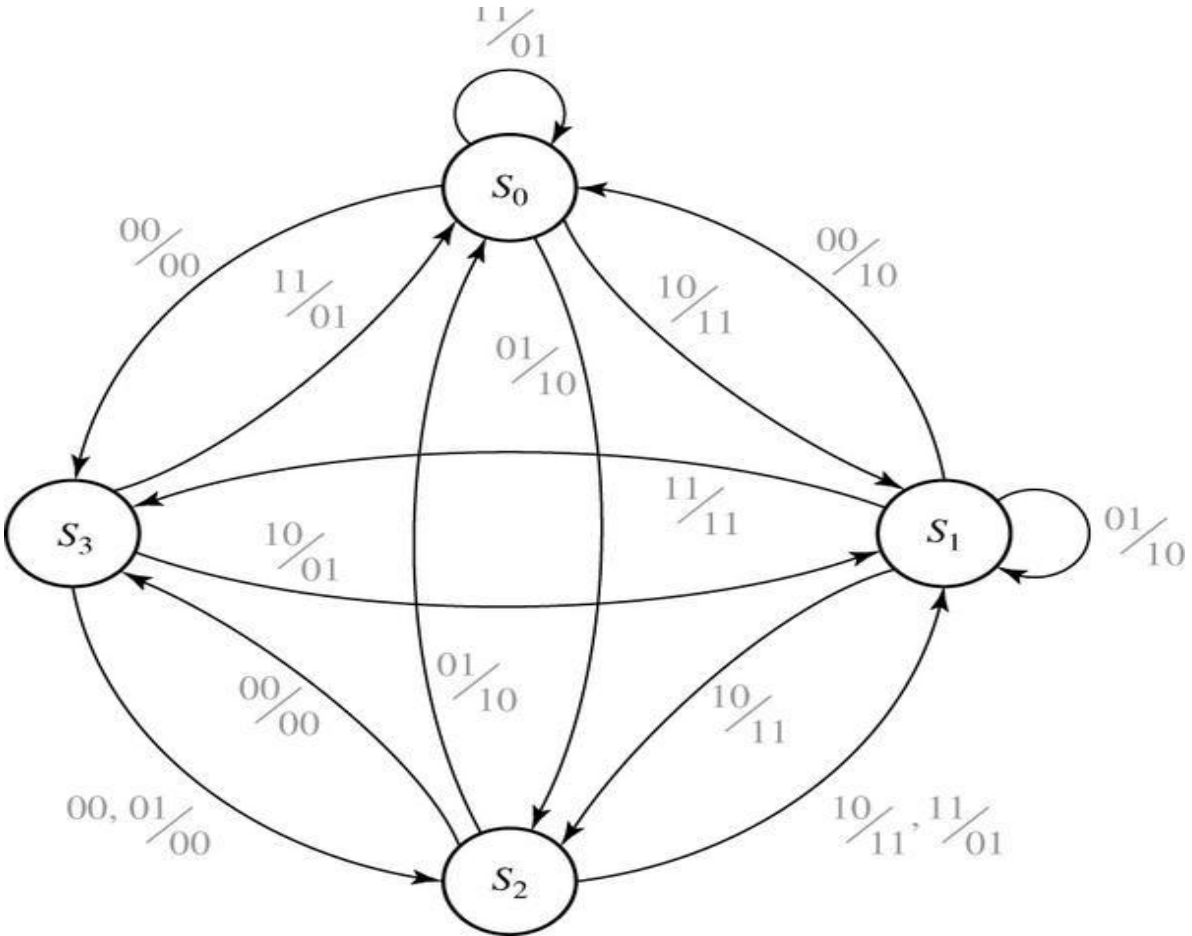
(b) Truth table

Multiple Inputs/Outputs

- **00,01/00 means if $X_1 = X_2 = 0$ or $X_1 = 0$ and $X_2 = 1$, then $Z_1 = 0$ and $Z_2 = 0$.**

TABLE 13-4
A State Table with Multiple Inputs and Outputs

Present State	Next State X_1X_2 = 00	01	10	11	Present Output (Z_1Z_2) X_1X_2 = 00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01



Timing Chart

- State change occurs after the falling (rising) edge of the clock.
- Input will normally be stable immediately before and after the active clock edge.
- For a Moore circuit, the output changes only when the state changes.
- For a Mealy circuit, the output can change when the input changes and when the state changes.

Timing Charts (cont.)

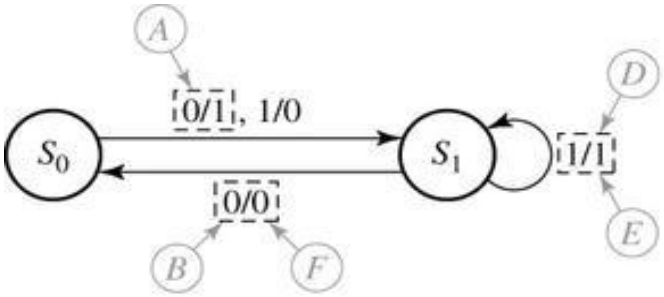
- For a Mealy circuit, a false output may occur between the time the state changes and the time the input is changed.
  - If the state has changed to its next value, but the old input is still present, the output may be temporarily incorrect.
  - False outputs are difficult to determine from the state graph.
    - Use signal tracing or
    - Use the state table.

Timing Chart Constructions

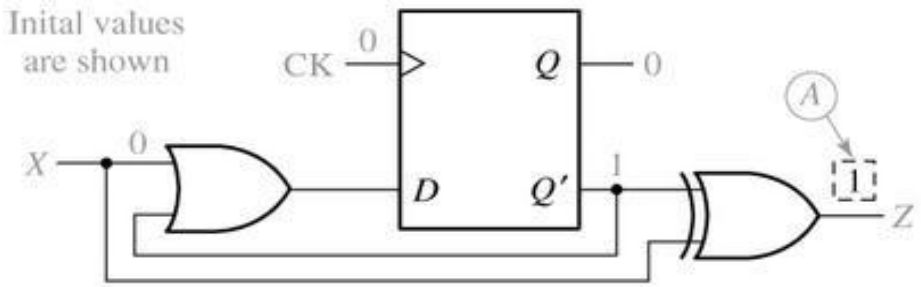
- Procedures: using a Mealy state table to construct a timing chart (given an input sequence).
  - For the first input, read the present output and plot it.
  - Read the next state and plot it (following the active edge of the clock).
  - Go to the row in the table which corresponds to the next state and read output under the old input column and plot it. (This may be a false output.)
  - Change to the next input and repeat
- For a Mealy circuit, the best time to read the output is just before the active edge of the clock.

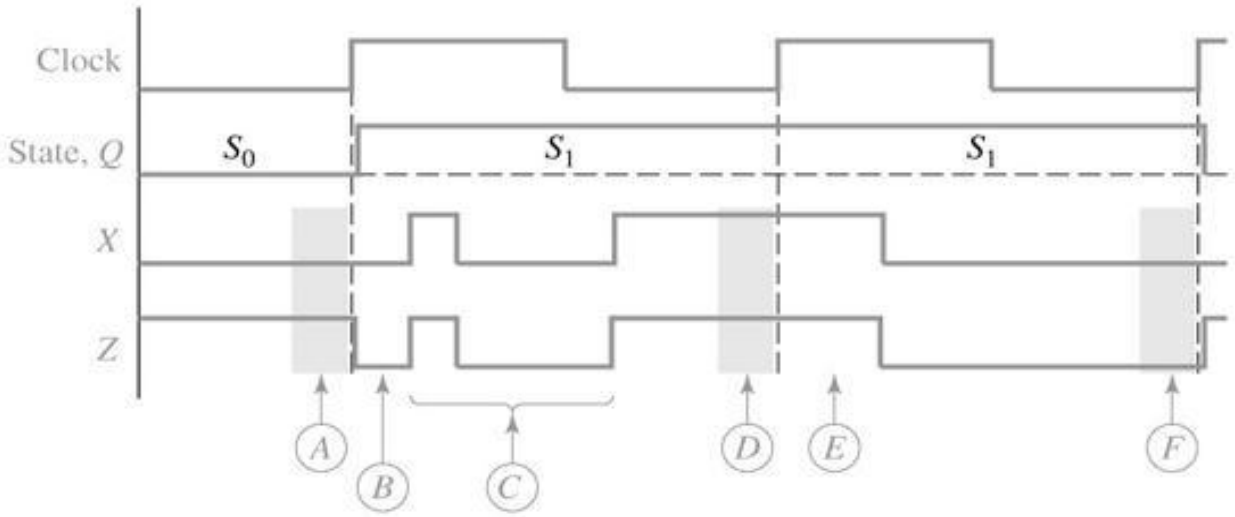
Interpretation of Timing Chart

- Read output before the rising edge of the clock.



Q		X = 0	1	0	1
0	S_0	S_1	S_1	1	0
1	S_1	S_0	S_1	0	1

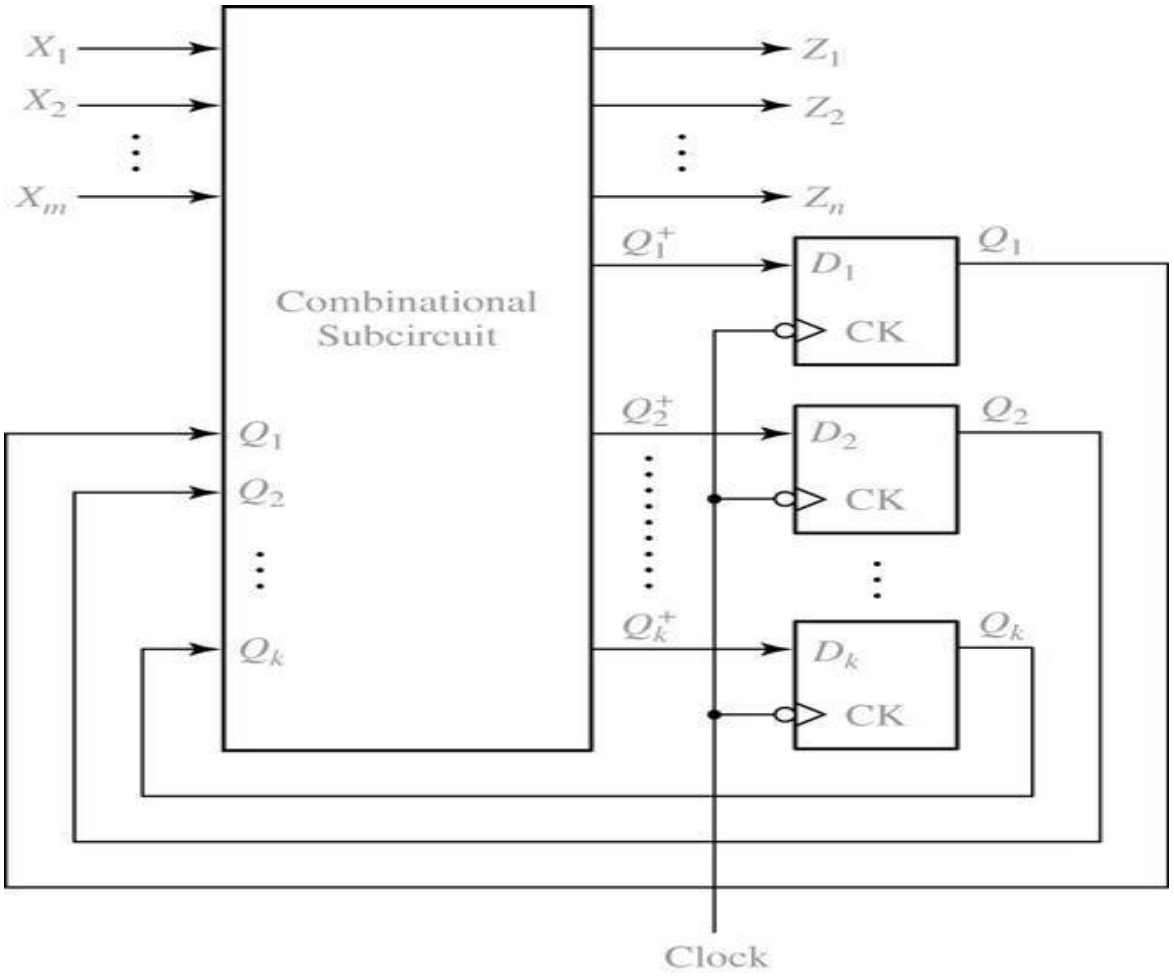




Read X and Z in shaded area (before rising edge of clock).

General Model

- Mealy network using D FF

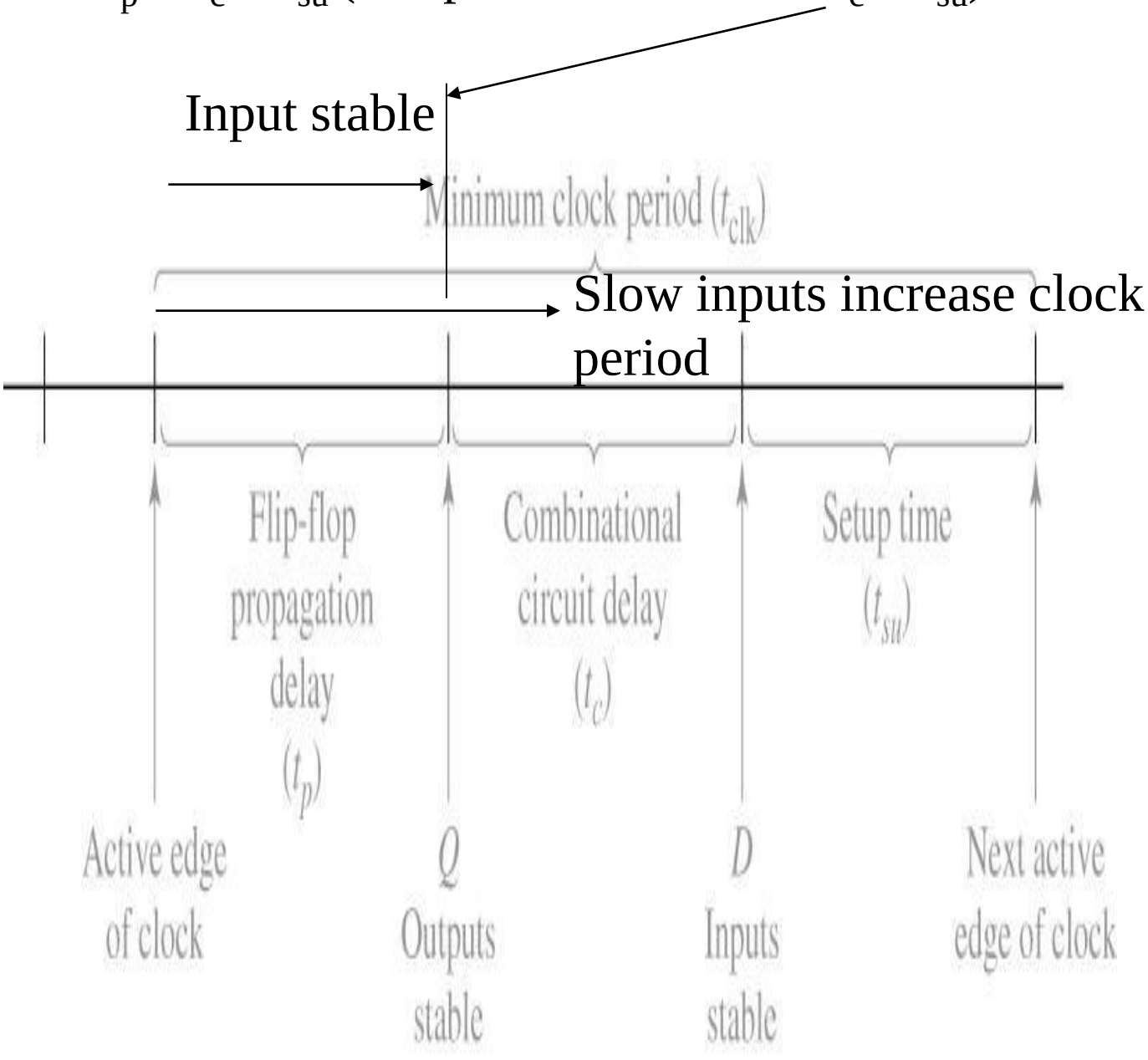


$$\left.\begin{aligned} Z_1 &= f_1(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \\ Z_2 &= f_2(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \\ &\vdots \\ Z_n &= f_n(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \end{aligned}\right\} n \text{ output functions}$$

$$\left.\begin{aligned} Q_1^+ = D_1 &= g_1(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \\ Q_2^+ = D_2 &= g_2(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \\ &\vdots \\ Q_k^+ = D_k &= g_k(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \end{aligned}\right\} k \text{ next-state functions}$$

Clock Period

- Minimum clock period for Mealy circuit = $t_p + t_c + t_{su}$ (if inputs stable before $t_c + t_{su}$)



General Model

- Moore network using D FF
  - Outputs are only a function of the present state of the FFs and not a function of the inputs.