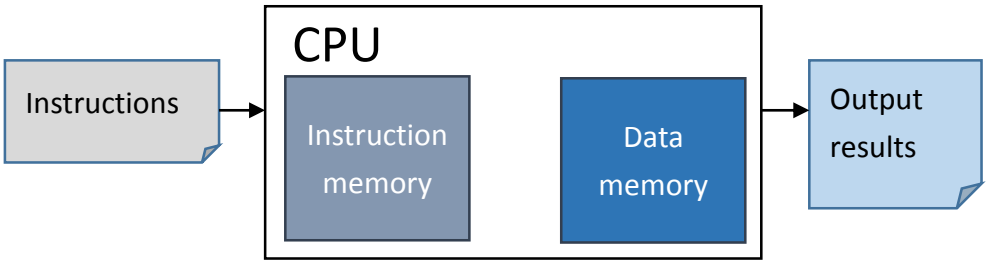
2015 Spring Logic System

Assignment 2 – A Simple CPU

1. Purpose:

To have a basic understanding in Central Processing Unit (CPU) by designing a preliminary CPU.

2. A simple diagram of CPU:



3. Specification of CPU:

1) 8-bit address

2) 4 general purpose registers and 1 program counter (all 8-bit)

3) Single-cycle (1 instruction is resolved in 1 cycle)

4. Instruction Set Architecture (ISA):

imm is short for immediate, Sel is short for select, Addr is short for address

See Note for detailed explanation of every instructions.

Instructions	OP code	Format	Description
MOV Rd, imm	001	[7:5] [4:3] [2:0]	Rd = imm
		[OP] [Rd] [imm]	
ADD Rd, Rs	010	[7:5] [4] [3:2] [1:0]	Rd = (Sel == 0) ?
		[OP] [Sel] [Rd] [Rs/imm]	Rd + Rs : Rd + imm
SUB Rd, Rs	011	[7:5] [4] [3:2] [1:0]	Rd = (Sel == 0) ?
		[OP] [Sel] [Rd] [Rs/imm]	Rd – Rs : Rd - imm
LD Rd, [Rs]	100	[7:5] [4] [3:2] [1:0]	Rd = (Sel == 0) ?
		[OP] [Sel] [Rd] [Rs/Addr]	[Rs] : [Addr]
ST Rd, [Rs]	101	[7:5] [4] [3:2] [1:0]	If Sel == 0, [Rs] = Rd
		[OP] [Sel] [Rd] [Rs/Addr]	Else [Addr] = Rd
BRA Offset	110	[7:5] [4:0]	New PC
		[OP] [Offset]	= current PC + offset

5. I/O Specification:

1) CPU should be compiled as executable file and read a file called input.txt without asking users to input the file's name.

2) input.txt contains the instructions being executed in binary format with no mark.

3) CPU should output a file called output.txt after it finishes all operations.

4) output.txt contains the content of **data memory**, **registers** and **program counter** in binary and decimal (2's complement except program counter).

Example of input.txt:

```
00100100
00101001
01000001
```

Example of output.txt:

```
MEM[0] = 00000001
MEM[1] = 00000000
MEM[2] = 00001000
…
MEM[255] = 00000010
REG[0] = 00100001
REG[1] = 00011111
REG[2] = 00001100
REG[3] = 10000000
PC = 00010000
```

The output doesn't need to be the same as the example, but it should be readable and clear.

6. Note:

1) When the CPU starts working, program counter is initialized to 0.

2) 8-bit is considered a byte. The memory in this system is byte-addressable.

Memory

address	value
0	xxxxxxxx
1	xxxxxxxx
2	xxxxxxxx

3) BRANCH's operation is pc-relative, which means the new pc is the result of current pc adds offset (2's complement).

4) For ADD/ SUB, if Sel is 0, use the values stored in registers to performance operations, otherwise treat Rs as immediate value and use it directly to do calculation.

5) For LD/ ST, if Sel is 0, use the value stored in Rs as address to access memory, otherwise treat Rs as address and use it directly to access memory.

7. Document Requirement

1) program execution flow

2) your review of this assignment

3) whatever you want to tell TA about this assignment

8. Homework Submission

1) Due day: 06/19 11:59 p.m.

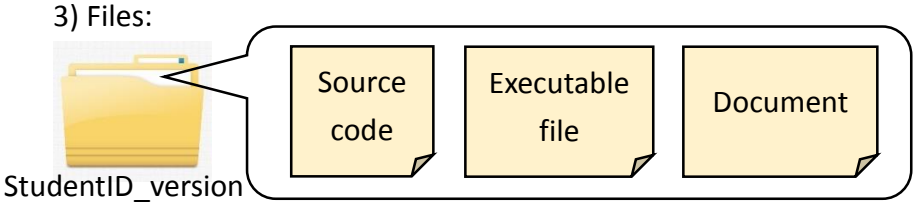
2) FTP:

FTP site: 140.116.164.252

user name: logic_lab

password: logic2015

3) Files:



9. TA Information:

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