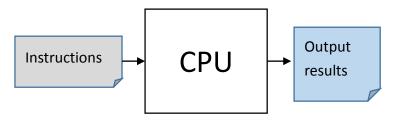
2015 Spring Logic System

Assignment 2 – A Simple CPU

1. Purpose:

To have a basic understanding in Central Processing Unit (CPU) by designing a preliminary CPU.

2. A simple diagram of CPU:



3. Specification of CPU:

- 1) 8-bit address
- 2) 4 general purpose registers and 1 program counter (all 8-bit)
- 3) Single-cycle (1 instruction is resolved in 1 cycle)

4. Instruction Set Architecture (ISA):

Instructions	OP code	Format	Description
MOV Rd, imm	001	[7:5] [4:3] [2:0]	Rd = imm
		[OP] [Rd] [imm]	
ADD Rd, Rs	010	[7:5] [4] [3:2] [1:0]	Rd = Rd + Rs
		[OP] [0] [Rd] [Rs]	
SUB Rd, Rs	011	[7:5] [4] [3:2] [1:0]	Rd = Rd – Rs
		[OP] [0] [Rd] [Rs]	
LD Rd, [Addr]	100	[7:5] [4:3] [2:0]	Rd = [Addr]
		[OP] [Rd] [Addr]	
ST Rs, [Addr]	101	[7:5] [4:3] [2:0]	[Addr] = Rs
		[OP] [Rd] [Addr]	
BRA Offset	110	[7:5] [4:0]	New PC
		[OP] [Offset]	= current PC + offset

5. I/O Specification:

- 1) CPU should be compiled as executable file and read a file called input.txt without asking users to input the file's name.
- 2) input.txt contains the instructions being executed in binary format with no mark.
- 3) CPU should output a file called output.txt after it finishes all operations.
- 4) output.txt contains the content of memory, registers and program counter in binary and decimal (2's complement except program counter).

Example of input.txt:

00100100 00101001 01000001

Example of output.txt:

MEM[0] = 00000001
MEM[1] = 00000000
MEM[2] = 00001000
...
MEM[63] = 00000010
REG[0] = 00100001
REG[1] = 00011111
REG[2] = 00001100
REG[3] = 10000000
PC = 00010000

The output doesn't need to be the same as the example, but it should be readable and clear.

6. Note:

1) 8-bit is considered a byte. The memory in this system is byte-addressable.

Memory

address	value	
0	xxxxxxx	
1	xxxxxxx	
2	xxxxxxx	

2) BRANCH's operation is pc-relative, which means the new pc is the result of current pc adds offset (2's complement).

7. Document Requirement

- 1) program execution flow
- 2) your review of this assignment
- 3) whatever you want to tell TA about this assignment

8. Homework Submission

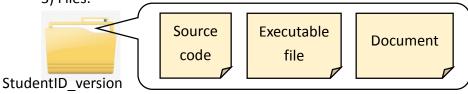
1) Due day: 06/19 11:59 p.m.

2) FTP:

FTP site: 140.116.164.252

user name: logic_lab password: logic2015





9. TA Information:

Name: 謝宛珊

e-mail: vanaheim.wen@gmail.com

Lab: 92617