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Myriad 2:

"Eye of the Computational Vision Storm"

David Moloney, Co-founder & CTO

Co-Authors: Brendan Barry, Richard Richmond, Fergal Connor, Cormac Brick, David Donohoe, et al.

Hot Chips 26   August 12, 2014

Movidius Update Since Hot Chips 2011

- Mobile Vision Processor company opening the era of computational cameras:

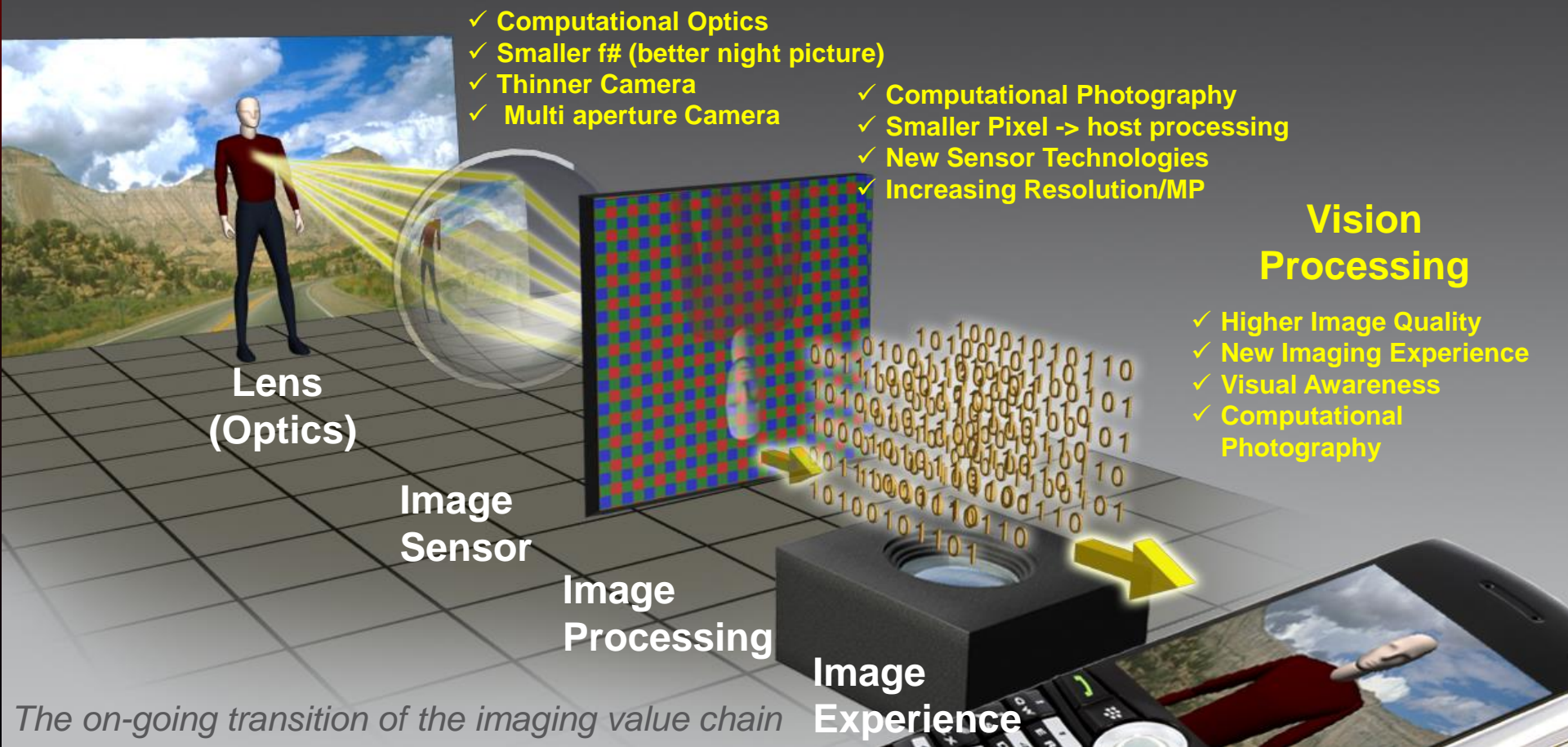SLR performance in mobile devices

Brand new UXP for mobile devices

Brand new product categories

- 8+ years of heritage. Close to $60M invested into technology development
- Proven architecture. 100% internally developed. Strong IP position
- February 2014 announcement: Google partnership with Myriad 1
- July 30, 2014 announcement: Myriad 2 Vision Processor SOC
- Headquartered in San Mateo, CA with design centers in Dublin, Ireland and Timisoara, Romania. Currently employing 70 staff including 65 engineers (10% hardware, 90% software/system)

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Disruptive Imaging Evolution
From <u>Digital</u> Imaging to <u>Computational</u> Imaging

✓ **Computational Optics**
✓ **Smaller f# (better night picture)**
✓ **Thinner Camera**
✓ **Multi aperture Camera**

✓ **Computational Photography**
✓ **Smaller Pixel -> host processing**
✓ **New Sensor Technologies**
✓ **Increasing Resolution/MP**

Vision Processing

✓ **Higher Image Quality**
✓ **New Imaging Experience**
✓ **Visual Awareness**
✓ **Computational Photography**

Lens (Optics)

Image Sensor

Image Processing

Image Experience

The on-going transition of the imaging value chain

Why Digital → Computational Imaging ?
the only way to overcome physical, mechanical and computational limitations of today's mobile cameras

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Why are Computational Cameras a Game Changer ?
Highway to the next generation user experiences
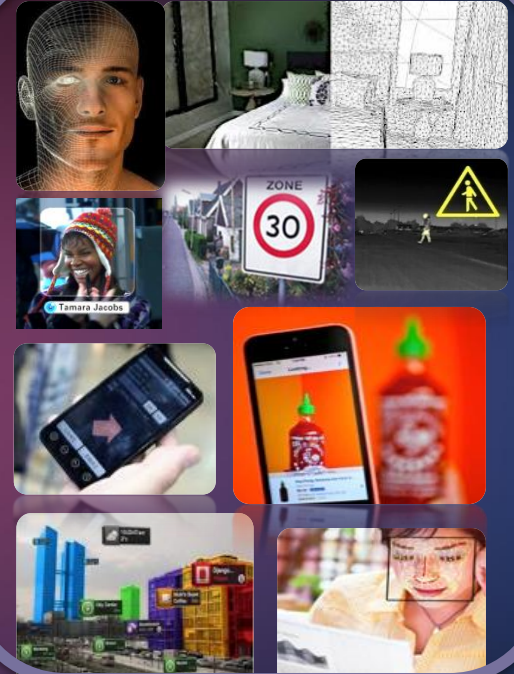
Image Capture

Computational Photography

Visual Awareness

Image Capture
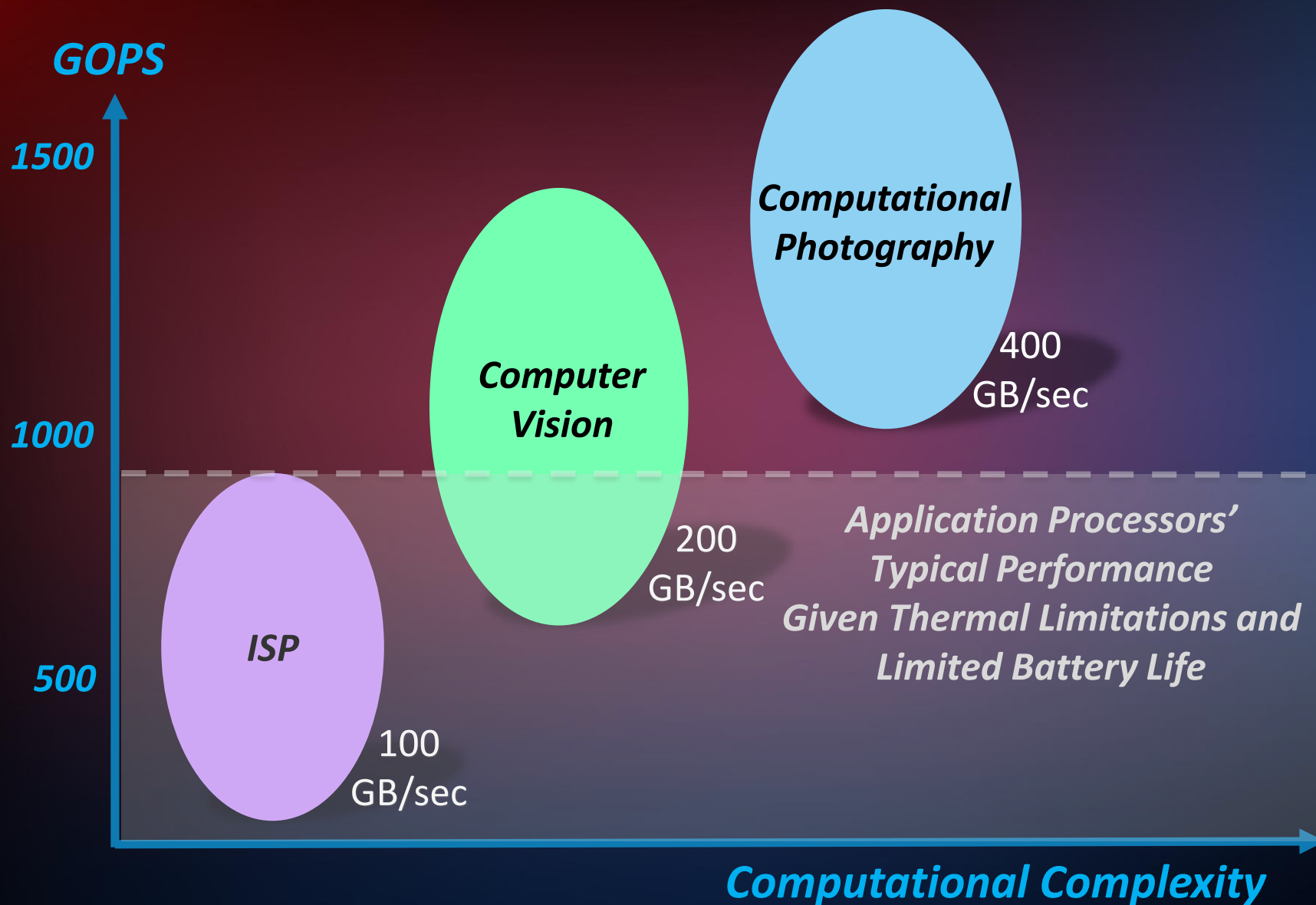
"Optical" zoom, Depth, HDR, Ultra-fast AutoFocus, Panorama, 360º capture, Extreme low light

3D Modeling, 3D Scanning, Visual Search, Indoor navigation, Augmented reality, Object detection, Object recognition…

The old paradigm

Vision Processing: the new imaging paradigm

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Need for Special Purpose Vision Processor

GOPS

1500

1000

500

Computational Photography
400 GB/sec

Computer Vision
200 GB/sec

ISP
100 GB/sec

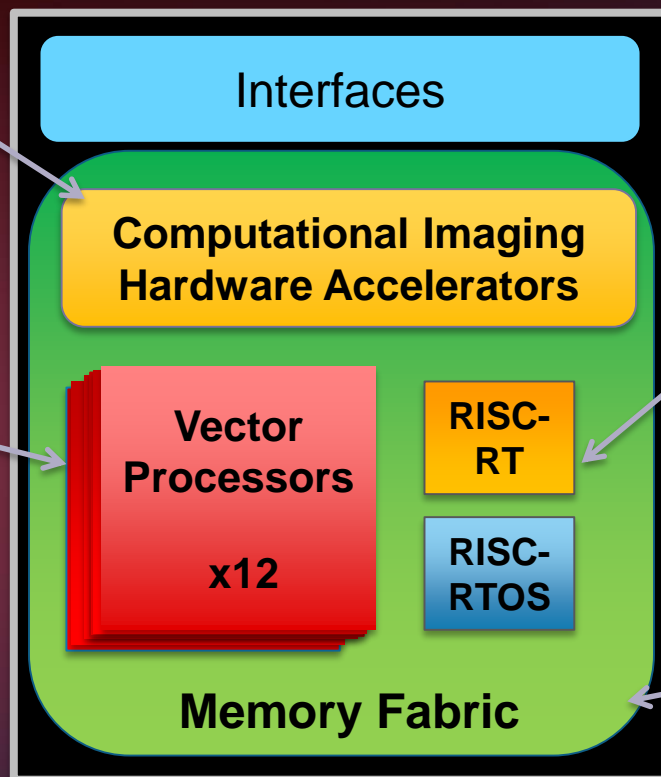*Application Processors' Typical Performance Given Thermal Limitations and Limited Battery Life*

Computational Complexity

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Introducing the Myriad 2 Vision Processor SOC

Optimized **configurable** imaging and vision hardware engines (framework)

Vector VLIW processors designed to crunch complex vision and imaging algorithms at high performance and low power
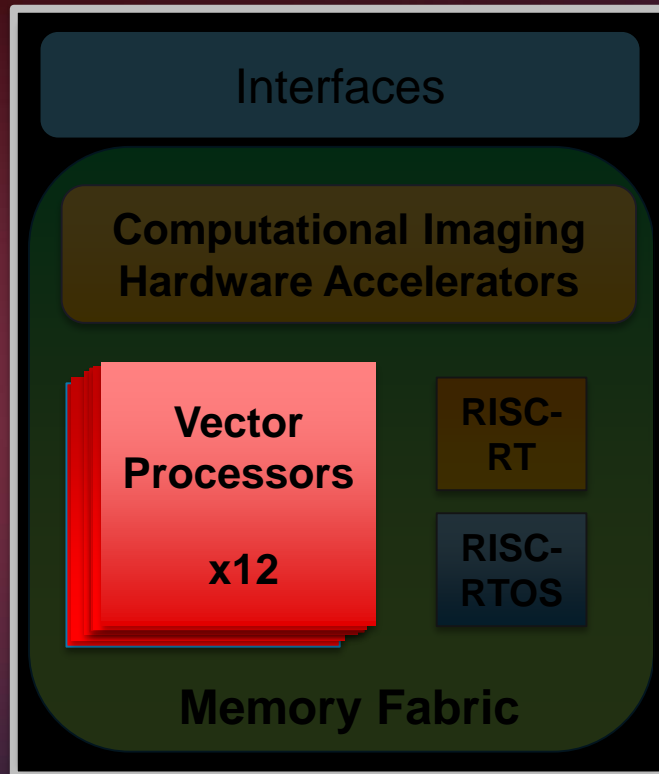
Interfaces

Computational Imaging Hardware Accelerators

Vector Processors

x12

RISC-RT

RISC-RTOS

Memory Fabric

RISCs run RTOS, Firmware, RunTime Scheduler…

Memory designed for low power, zero latency, sustained high performance through **data locality**
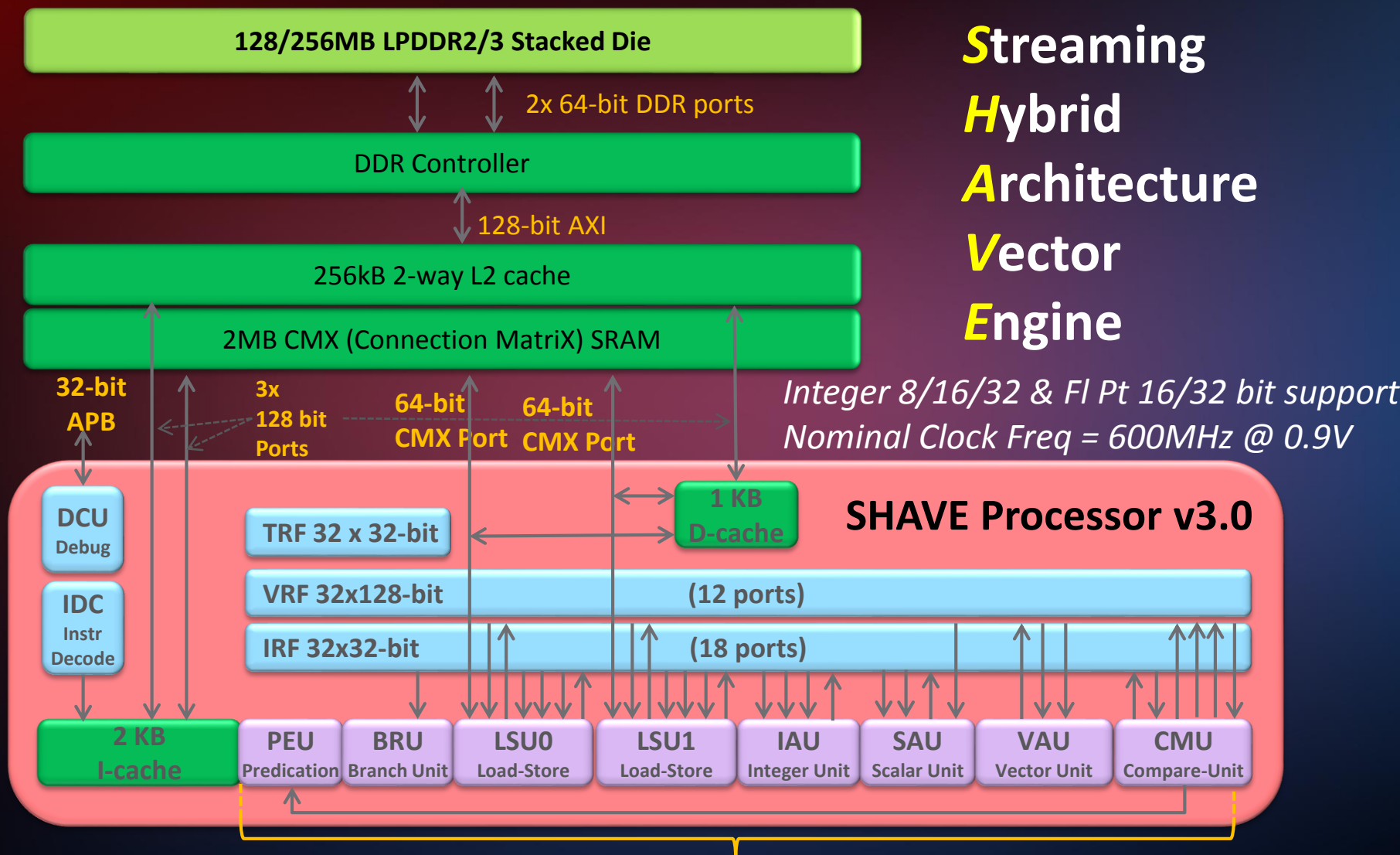
Nominal 600 Mpixels/sec throughput enables connection to multiple cameras, world-class computational imaging pipelines, and complex vision applications

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(1) Specialized Vector VLIW Processors for Vision

Interfaces

Computational Imaging Hardware Accelerators

Vector Processors

x12

RISC-RT

RISC-RTOS

Memory Fabric

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SHAVE 128 bit SIMD-VLIW Vector Processors

128/256MB LPDDR2/3 Stacked Die

2x 64-bit DDR ports

DDR Controller

128-bit AXI

256kB 2-way L2 cache

2MB CMX (Connection MatriX) SRAM

32-bit APB

3x 128 bit Ports

64-bit CMX Port

64-bit CMX Port

SHAVE Processor v3.0

DCU Debug		TRF 32 x 32-bit			1 KB D-cache	

VRF 32x128-bit — (12 ports)

IRF 32x32-bit — (18 ports)

IDC Instr Decode

2 KB I-cache	PEU Predication	BRU Branch Unit	LSU0 Load-Store	LSU1 Load-Store	IAU Integer Unit	SAU Scalar Unit	VAU Vector Unit	CMU Compare-Unit

Streaming
Hybrid
Architecture
Vector
Engine

Integer 8/16/32 & Fl Pt 16/32 bit support
Nominal Clock Freq = 600MHz @ 0.9V
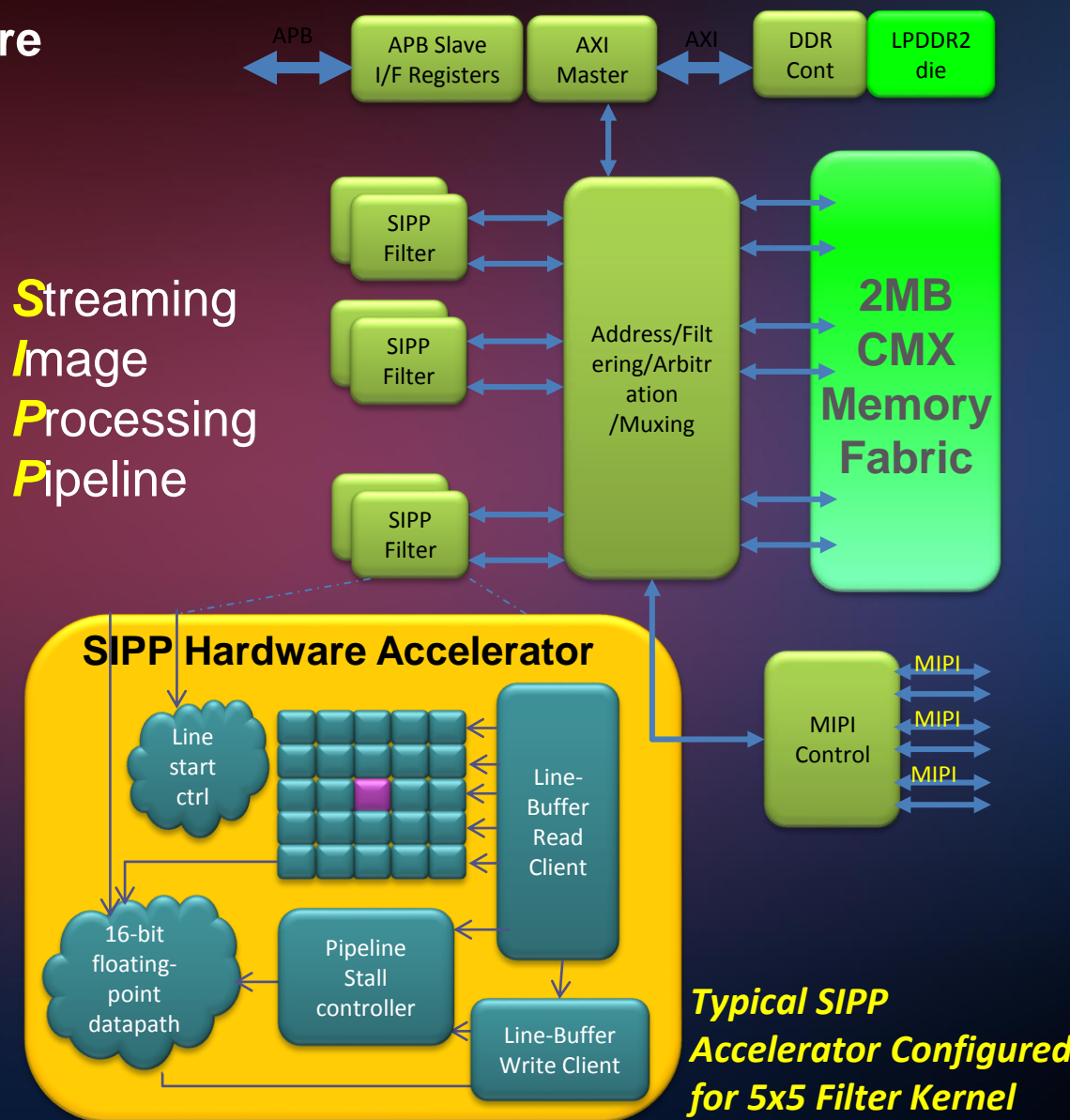
8 parallel SHAVE VLIW Functional Units Supplied with VRF & IRF Data
128-bit Instruction-Fetch (Variable-Length Instructions max 192 bits)

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(2) Imaging Hardware Accelerators
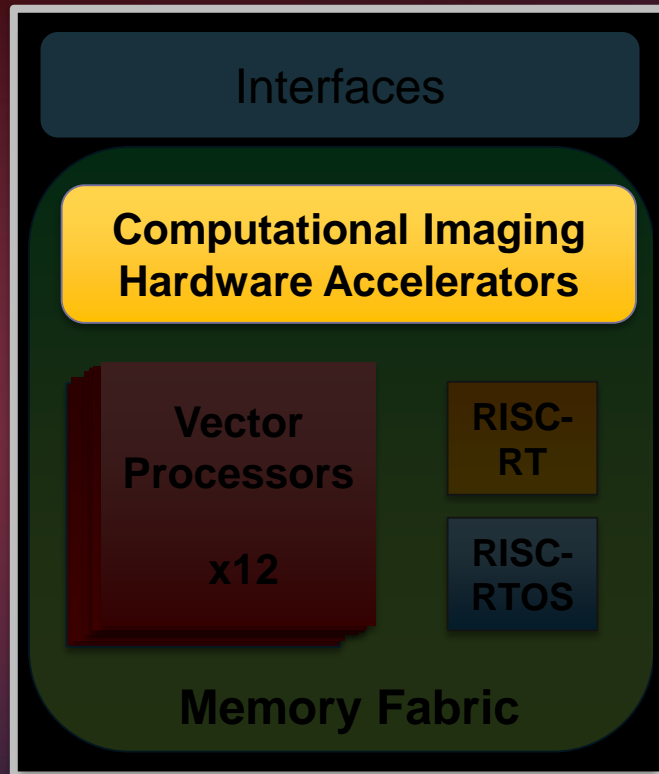
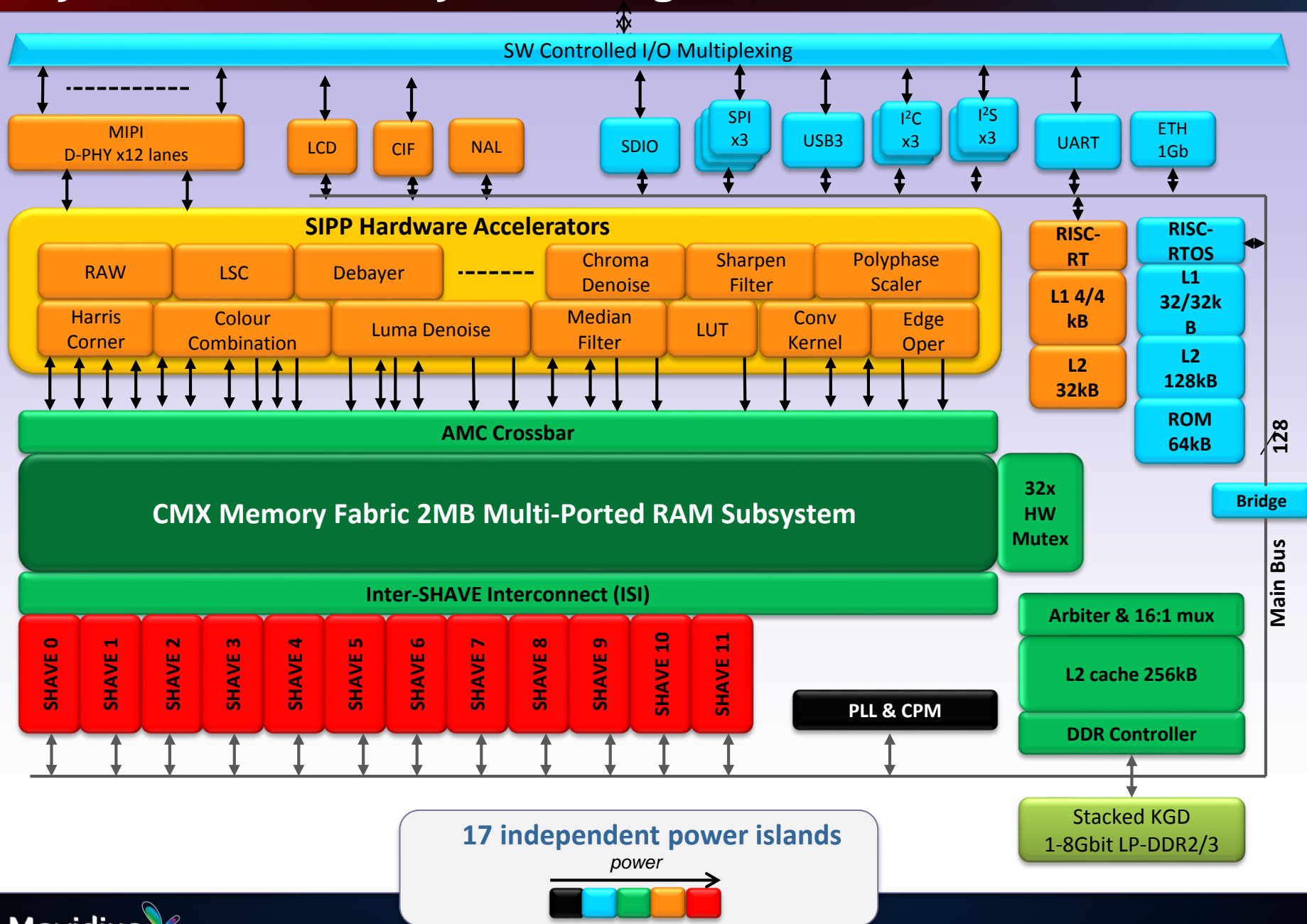# SIPP Computational Imaging Hardware Accelerators

- **20+ programmable hardware accelerators including:**
  - **Poly-phase resizer**
  - **Lens shading correction**
  - **Harris Corner detector**
  - **HoG/Edge operator**
  - **Convolution filter**
  - **Sharpening filter**
  - **γ correction**
  - **tone-mapping**
  - **Luma/Chroma Denoise**
  - **..and others**

- **Each accelerator has**
  - **Memory ports**
  - **Local decoupling buffers**
  - **Ability to fully compute 1 operation per pixel per cycle**

Streaming
Image
Processing
Pipeline

APB

APB Slave I/F Registers	AXI Master

AXI

DDR Cont	LPDDR2 die

SIPP Filter

SIPP Filter

SIPP Filter

Address/Filtering/Arbitration/Muxing

2MB CMX Memory Fabric

SIPP Hardware Accelerator

Line start ctrl

Line-Buffer Read Client

16-bit floating-point datapath

Pipeline Stall controller

Line-Buffer Write Client

MIPI Control

MIPI

MIPI

MIPI

Typical SIPP Accelerator Configured for 5x5 Filter Kernel

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SIPP Hardware Accelerators Details
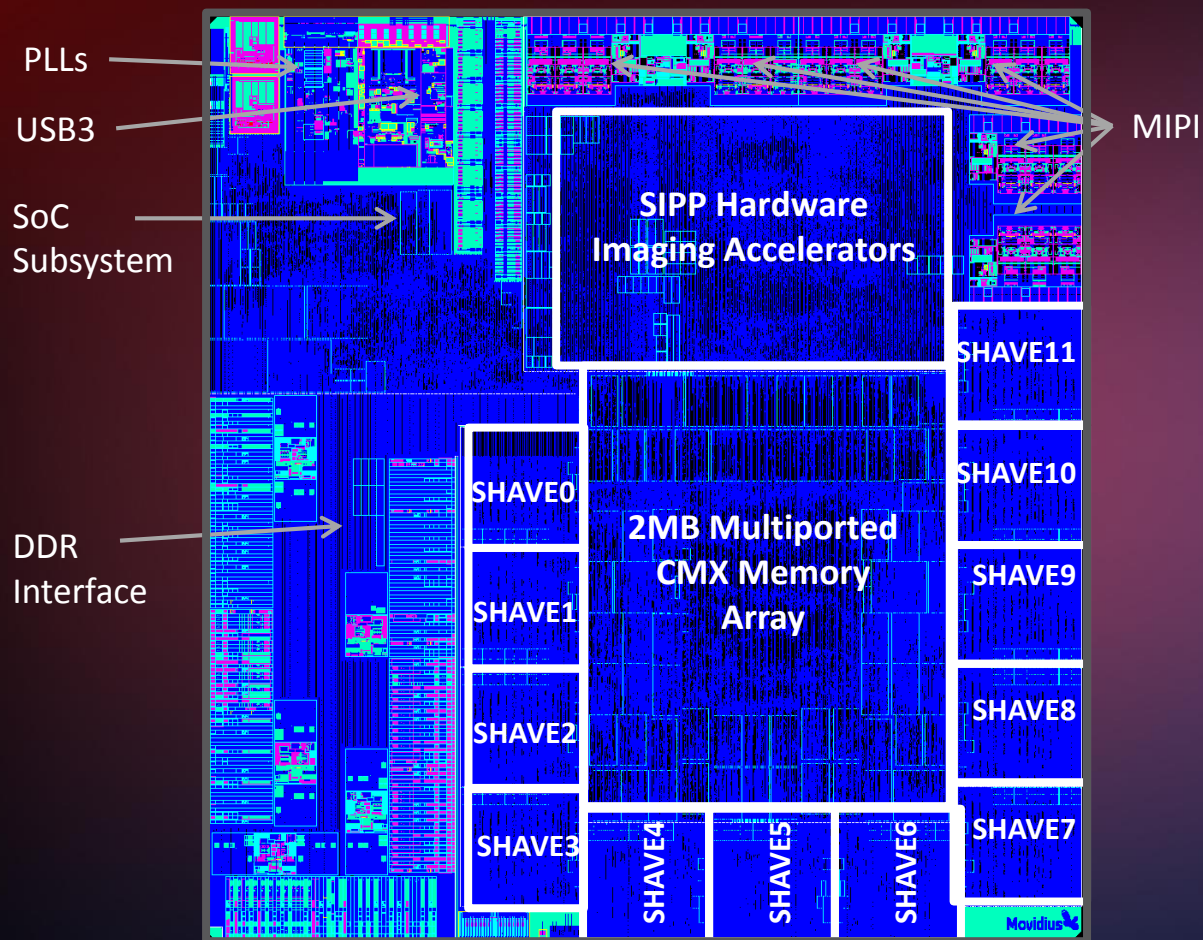
- Myriad 2 achieves **20-30x** performance of Myriad 1
  - SHAVE performance compared to Myriad 1 roughly: (600 MHz / 180 MHz) * (12/8) = **5x**
  - SIPP Hardware Accelerators in Myriad 2 can output one fully computed output pixel per cycle
    - Comparison with SHAVE-only software filters on Myriad 1 which range from 1.5 up to dozens of cycles per pixel
    - **15-25x** additional performance compared to Myriad1

- Hardware accelerator rationale fits with Moore's law trend below 28nm
  - Memory access is expensive in terms of power
  - Memory scaling 20-30% vs 50% for logic
  - This means we can trade arithmetic OPS for less memory occupancy and lower power

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Myriad 2 Detailed System Diagram

SW Controlled I/O Multiplexing

MIPI D-PHY x12 lanes | LCD | CIF | NAL | SDIO | SPI x3 | USB3 | I²C x3 | I²S x3 | UART | ETH 1Gb

SIPP Hardware Accelerators

| RAW | LSC | Debayer | - - - - - - - | Chroma Denoise | Sharpen Filter | Polyphase Scaler |

| Harris Corner | Colour Combination | Luma Denoise | Median Filter | LUT | Conv Kernel | Edge Oper |

RISC-RT
L1 4/4 kB
L2 32kB

RISC-RTOS
L1 32/32kB
L2 128kB
ROM 64kB

AMC Crossbar

CMX Memory Fabric 2MB Multi-Ported RAM Subsystem

32x HW Mutex

128

Bridge

Main Bus

Inter-SHAVE Interconnect (ISI)

SHAVE 0 | SHAVE 1 | SHAVE 2 | SHAVE 3 | SHAVE 4 | SHAVE 5 | SHAVE 6 | SHAVE 7 | SHAVE 8 | SHAVE 9 | SHAVE 10 | SHAVE 11

Arbiter & 16:1 mux

L2 cache 256kB

DDR Controller

PLL & CPM

Stacked KGD 1-8Gbit LP-DDR2/3

17 independent power islands

power

Myriad 2 Die

TSMC 28 nm HPM process
6.5mm x 6.5mm
0.4mm pitch
BGA

1Gbit
LPDDR2
1x32bit
532 MHz

Myriad 2 Die, No DDR
5.1mm x 5.3mm
0.35mm pitch
WLCSP

PLLs

USB3

SoC
Subsystem

DDR
Interface

MIPI

SIPP Hardware
Imaging Accelerators

SHAVE11

SHAVE10

SHAVE0

2MB Multiported
CMX Memory
Array

SHAVE9

SHAVE1

SHAVE8

SHAVE2

SHAVE9

SHAVE3 SHAVE4 SHAVE5 SHAVE6 SHAVE7

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Myriad 2 Software Development Kit (MDK)

Reference Application Examples	Movidius Partners **Applications**	**MoviTools**
Frameworks (Graph API Construction, OpenCL)		**IDE**

LAMA Linear Algebra Library	**MV CV** Vision Library	**MV ISP** Imaging Library	Movidius Partners **Libraries**	**Compiler Assembler Simulator Profiler**

Board Support Package (BSP)

MV182 Development Board Hardware
(with Myriad 2 Vision Processor SOC)

Debugger

- Powerful frameworks for efficient application development
- Efficient tools
- Rich set of libraries and applications
- Movidius partners ecosystem

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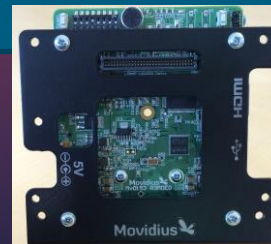
Myriad 2 Power Efficiency: Depth Extraction

- Depth extraction using structured light
  - Projector emits structured light pattern
  - Aligned camera captures reflected structured light pattern
  - Significant computation required to extract depth

- Achieves 30 fps < 250 mW full package power

- Resources used on Myriad 2:
  - 6 x SHAVE vector VLIW processors
  - 2 x SIPP hardware accelerators
  - Mix of 16b floating-point intermediates and 32b floating-point final output

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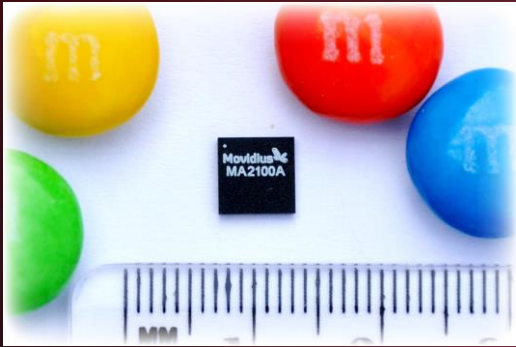# Hard Real-time Support for Low Latency Computer Vision

- Essential for line sync based super low latency processing
- Deterministic data access due to 2MB on-chip SRAM
  - And dedicated stacked DDR (no contention with GPU etc.)
- Low latency (<2μsec worst case) interrupt handling
  - No contention with peripherals such as USB, SPI etc.
- 64 bit timestamp support

Algorithm Example	Details
Haar Cascade classification	OpenCV compatible multi-scale Haar Cascade with 20 stages, computed using 12 x SHAVEs and 1 x SIPP accelerator. **Latency:** For each 1080p resolution frame, calculates 50,000 multi-scale classifications in <7 msec

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Conclusions

- **We're entering a new era of computational imaging**

- **Myriad 2: An advanced 28nm self-contained Vision Processor SOC**
  - Aggregate nominal 600 Mpixel/sec throughput for complete pipeline(s)
  - Sustained performance from a highly innovative multicore memory subsystem (400GB/sec BW)
  - Low-latency for demanding vision applications by allowing flexible memory allocation lines, tiles etc. not just frames
  - 20-30x more performance per Watt compared to Myriad 1

- **Myriad 2 Software Development**
  - Powerful frameworks for efficient application development
  - Efficient tools
  - Rich set of libraries and applications
  - Movidius partners ecosystem

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